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Analysis of Local Bending Stress Effect on CMOS Performance Fabricated in Thinned Si Chip for Chip-to-Wafer 3D Integration

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1. Introduction

Three-dimensional LSI (3D-LSI) consisting of vertically stacked several thin LSI chips with lots of through-Si vias (TSVs) and metal microbumps has attracted much attention as a promising method to enhance performance of LSI [1]. Recently, great interests in electrical and mechanical reliability issues are increasing among 3D-LSI researches [2,3]. In conventional 3D-LSIs, metal microbumps that electrically connect upper and lower LSI chips are surrounded by organic adhesive called underfill material. The coefficient of thermal expansion (CTE) of the underfill material is larger than that of metal microbumps. As shown in Fig.1, this CTE mismatch induces local bending stress in thinned Si substrates after chip stacking. In addition, this local bending stress would affect MOSFET performance in Si chips [4]. In this paper, we have presented a new test structure to evaluate effects of local bending stress induced by CTE mismatch, and discussed those effects on CMOS inverter performance.

2. Experimental

The 3D-LSI test structure is composed of Si (dummy) microbumps, an underfill material, and a thinned Si chip/wafer stacked on Si substrate. Figurer 2 shows a schematic cross-section of 3D-LSI generating the local bending stress in a thinned chip/wafer due to the CTE mismatch between underfill material and Si microbumps. The structure was fabricated with following processes, as shown in Fig.3. First, Si microbumps were formed on Si substrate by inductively coupled plasma reactive ion etching (ICP-RIE). The bump size and height were 20 μm by 20 μm and 20 μm. The bump pitches were 50 μm. Then, the thinned Si chips were bonded on the Si substrate which was coated with an adhesive. In this paper, the thinned chip thickness was 30 μm. After that, epoxy used as the adhesive was additionally coated around the thinned chips. The chips-on-Si substrate was temporarily exposed in vacuum atmosphere and opened to the air to completely fill gaps between the thinned chips and the substrates by the epoxy. Finally, the epoxy was cured at 190 ℃ for 1 hour. This structure can give a tensile stress of more than 1 GPa to thinned Si chip [5]. After that, we measured the MOSFET and the CMOS inverter fabricated on the locally-bended thin Si chip.

3. Results and discussion

The simple chip-on-Si substrate structure with Si microbumps enables us to evaluate only local bending stress effects. First of all, we evaluated the impacts of local bending stress on the MOSFET characteristics. Figure 4 shows the layout of Si microbumps and MOSFETs in thinned Si chip. Both nMOSFET and pMOSFET were placed on points A and B, respectively. The drain current flowed along Y-axis direction. Figure 5 shows Id-Vd characteristics of nMOSFET and pMOSFET in thinned Si chip for both before and after bending the Si chip, where the Si substrate has 50-μm-pitch Si microbumps. By the local bending stress, ON current increased in both devices. These results agreed well with theoretical predictions. Actually, there were tensile strains around the point A, and there were also compressive stresses around the point B. It is well known that electron mobility increases by tensile strains and hole mobility increases by compressive stresses. Therefore, ON currents of both MOSFETs increase in accordance with the mobilities increase. Then we evaluated the CMOS inverter performance placed on point C, as shown in Fig. 6. Compressive stresses existed around the point C. Figure 7 shows measurement results of CMOS inverter under the compressive stress. This CMOS inverter consists of nMOSFET and pMOSFET with L_g/W_g of 0.22 μm/0.22 μm. Vsp means a voltage of inverter switching point depicted in a inset of Fig. 7, where the input voltage is equal to the output voltage. After bending, it was observed that the Vsp slightly increased. This result shows that compressive stress increased hole mobility and a resultant Vsp. Vsp is proportional to ratio β_p/β_n. Here, β_p and β_n are $\mu_p C_{ox} W_g/L_g$ and $\mu_n C_{ox} W_g/L_g$. It was clearly demonstrated that the local bending stress affects CMOS inverter, leading circuit performance fluctuations in the whole chip.

4. Conclusion

The effects of local bending stress applied to thinned Si chips were investigated in detail with the novel test structure that can generate controlled local bending stress by the CTE mismatch between underfill material and Si microbumps. The local bending stress affects the I-V characteristics of MOSFET and the switching behavior of the CMOS inverter. In order to realize higher performance 3D-LSIs with suppressing circuit performance degradation and fluctuation, careful design including layout of microbumps and MOSFETs is strongly required.

Acknowledgements

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References

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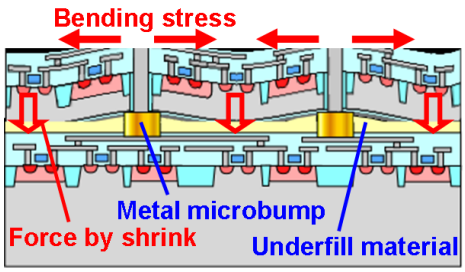

Fig. 1. Schematic cross-section of 3D-LSI expressing effects of local bending stress due to the CTE mismatch.

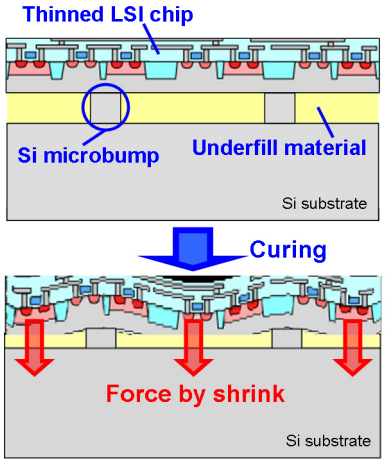

Fig. 2. Cross sectional schematic of proposed test structure having the local bending stress induced by CTE mismatch between underfill material and microbumps.

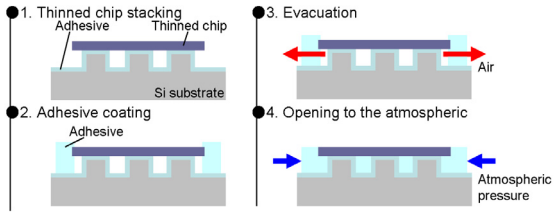

Fig. 3. Process flow of novel test structure.

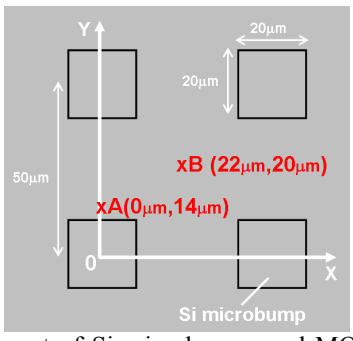

Fig. 4. Layout of Si microbumps and MOSFETs in thinned Si chip.

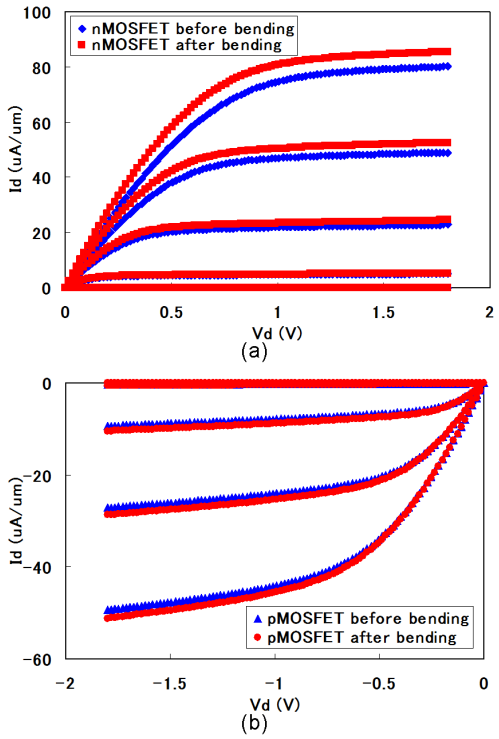

Fig. 5. Id-Vd characteristics of (a)nMOSFET, and (b)pMOSFET before and after bending.

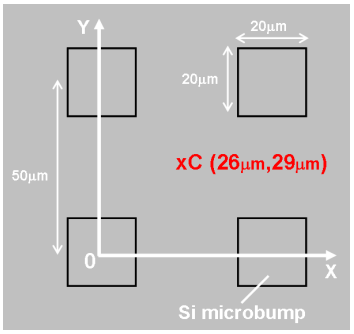

Fig. 6. Layout of Si microbumps and CMOS inverters in thinned Si chip.

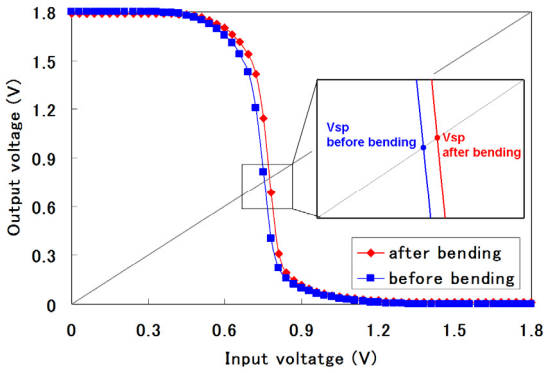

Fig. 7. CMOS inverter behaviors before and after bending.