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The results of self annealing process for a copper interconnection on the 4xnm DRAM Products

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Abstract

The DRAM products with a copper interconnection with larger grain size are preferred for lower electrical resistance and therefore better circuit performance. To characterize the evolution of the grain size, distribution and the metal line texture evolution during self annealing and DRAM process thermal budget with thermal excursion stress test. So we found out that condition with self annealing time affects its grain size and stress migration. This results is explained by the EBSD analysis and TOF-TEM

As compared to the conventional cu anneal process; no time delay, self annealing group show the more bamboo microstructure at dram damascene process.

In addition, we observed that enhanced thermal stress stability, which then results in lower hillock deformation to copper top surface after a batch furnace at 400℃, N_2 ambient in three Times.

Introduction

The DRAM process integration with electroplated copper interconnection enhanced the circuit delay performance. Generally, cu metallization is fabricated using the damascene process. The grain size and microstructure deformation of cu film are an important factors for dram process and product field application reliability.

In this study, we defined the effects of self annealing process to cu metallization for DRAM fabrication. And we will show the results of the self annealed cu films texture deformation, grain size distribution at pitched pattern and surface morphology [1-3]. It is therefore important to investigate the stress controlled copper process and mechanism of the micro texture evolution on the DRAM.

Experiment

The samples were prepared on 12 in. Si(100) wafers that had PECVD grown blank oxide layers. In this process, Ta Barrier layer with thickness of about 290Å with cu seed layers of 550Å thickness were deposited by PVD prior to electroplating. Especially, we are considered the different organic additive in EP Chemical: selected chemical 'A' and reference chemical 'B'.

To study the effect of self annealing process for dram product, thermal cycle stress test was performed on the self-annealed sample and others in a batch furnace at 400℃.

The plan view TEM technique was used for the grain boundary measurements and surface morphology observations. For the grain size distribution examinations in the pattern wafer, the EBSD (Electron Back Scattering Diffraction) analysis was used to measure grain size.

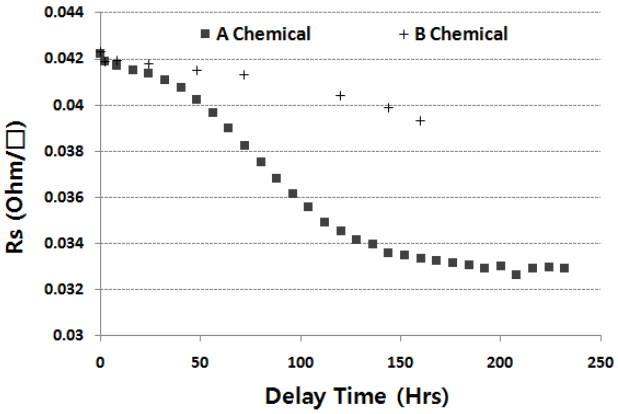

Fig. 1. Sheet resistance evolution during self-annealing of 0.5um film which of chemical 'A' and 'B' respectively.

Results and Discussion

For a typical, 0.5um thick copper film, the sheet resistance of a chemical 'A' is observed to drop by 20% within 160hrs after deposition at room temperature(Fig.1). Another was not. It seemed that a touch of influence of organic additives in these chemicals. In other words, chemical A has more driving forces for grain growth. At this point, we made full use of the phenomenon which of the reduction of time sheet resistance saturation time. Fig.2 presents a surface analysis of the copper microstructure after self-annealing or not. Self-annealed sample show the bigger grain size and no more grain growth than another sample with general annealing method. Fig.3 shows the cross-section views, self-annealed copper lines observed its bigger grain profile and it seems to be more bamboo structure. Then fig.4 shows a settle surface morphology with none of it; hillock profile, after the thermal excursion test which like to the DRAM Process thermal budget. Finally, we used special software to analyze the cu grain size distribution after DRAM processing, the top area of the Cu interconnect were measured by the EBSD, as shown in Fig.5,6 and Table.1 [4].

Conclusion

The self annealing effects in DRAM process show clear dependence on grain growth, size, and thermal stability. It would be helpful for DRAM to the initial stress relief and the lowest total energy change from (111) to (200) under thermally induced stress condition; Cu anneals and others dram thermal process integration. As the results of this study, we are awaking to the need for stress relieved cu annealing in DRAM process integration.

Finally we made good use these information where the manufacturing process for a graphic DRAM of the 2Gbit GDDR5 and DDR3 at 4xnm; keep delaying before cu anneal process.

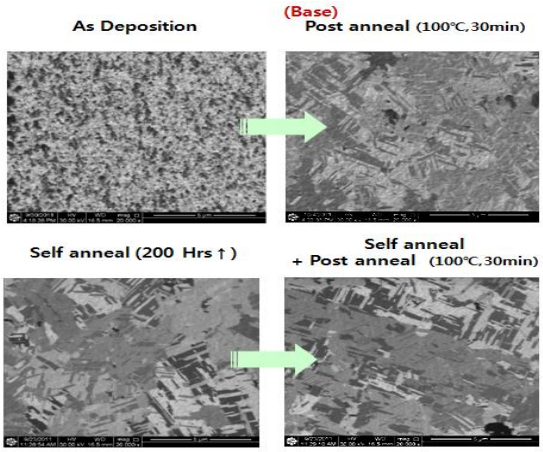

Fig.2. Planar TEM Image after the Post Treatment of Cu deposition

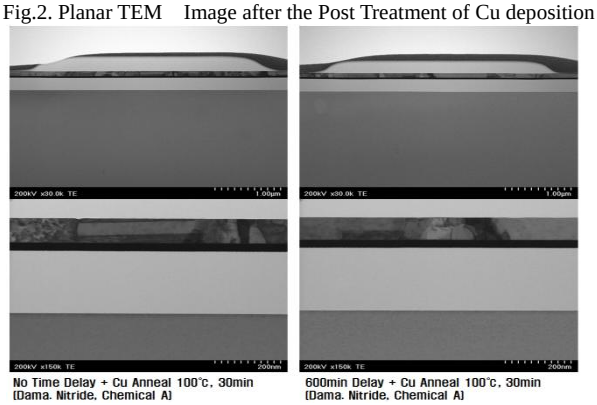

Fig. 3. Cu grain size profile after a self-annealing process

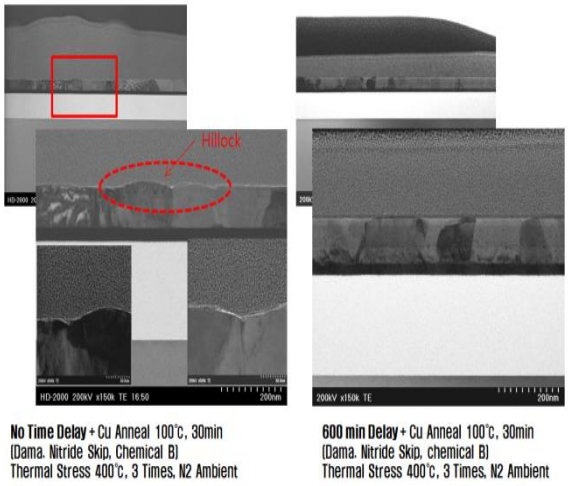

Fig. 4. Cu grain surface profile after thermal excursion test; Copper hillock observed the non-self annealing process but 600min delay sample is not.

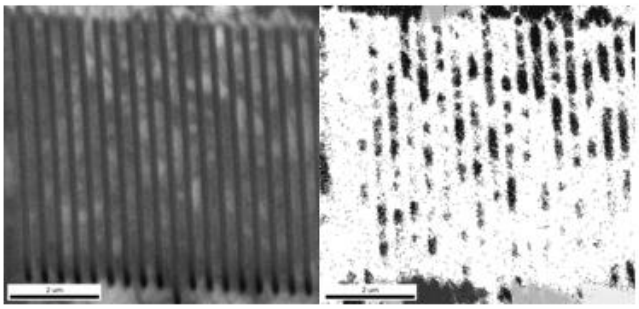

Fig. 5. A color map of the Cu Grain size using EBSD analysis; Chemical A, Cu Anneal 100℃, 30min. (No Time Delay; Industry standard)

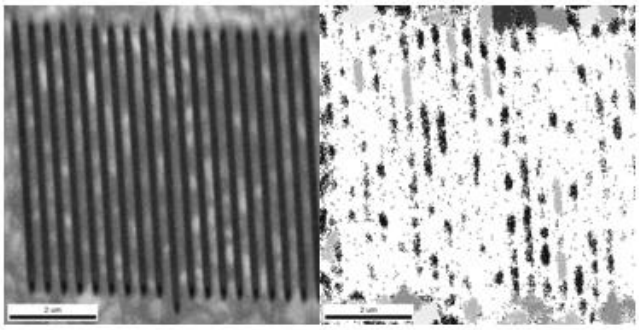

Fig. 6. A color map of the Cu Grain size using EBSD analysis; Chemical A, Cu Anneal 100℃, 30min.(Include 600 min time delay before cu annealing)

Grain Diameters (196nm width)	No Self-annealed		Self-Annealed (600min)	
	Number (ea)	Portion	Number (ea)	Portion
50nm under	3446	93.94	2156	86.97
50 ~ 100nm	103	2.808	161	6.494
100 ~ 150nm	31	0.845	54	2.178
150 ~ 200nm	22	0.599	38	1.532
200 ~ 500nm	61	1.663	62	2.501
500nm upper	5	0.136	8	0.323

Table 1. Summary of the numerical distribution in cu grain by the EBSD analysis technique; Chemical A

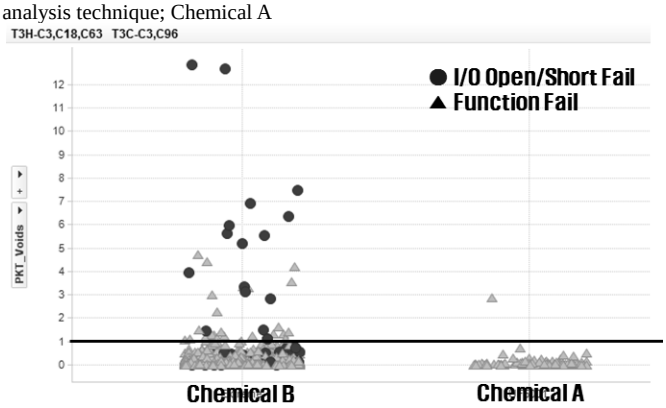

Fig.7. Package test results for open/short fail, I/O coupling pattern; the fail induced by copper voids

Reference

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