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# Current Enhancement of Green Transistors as Compare to Conventional Tunnel FETs with Dopant Segregated Process

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## 1. Introduction

A green transistor was proposed with modeling simulation by Prof. Hu of UC Berkeley since 2008 [1-6] for achieving steep switching behavior (SS < 60 mV/dec at room temperature) than the conventional MOSFET due to a gate-controlled band-to-band tunneling (BTBT) mechanism. However, the challenge for TFETs is to establish that their performance is superior to that of MOSFETs in increasing drive current. To increase the ON current without sacrificing the OFF current, a high-K dielectric with an integrated metal gate was included in the gate stack. Besides, the SOI substrate are widely used for TFETs fabrication process [7-11], which brought to the issues of cost and thermal dissipation for state-of-the-art process. In order to compatible with current process, this study demonstrates a p-type Tunneling FET (p-TFET) and p-type green FET (p-gFET) with Ni dopant segregation [9][12] at source and drain region on bulk Si (100) without SOI substrate, and an integrated high-K metal gate (HKMG) stack [13].

## 2. Devices Fabrication

Standard 6 inch MOS based line and gate last process are employed for this study. First, the $p^+$ and $n^+$ regions for drain and source were defined and implanted on p-type Si substrate (100), and were implanted by $BF_2$ (40keV, $4x10^{15}$ $cm^{-2}$) and P (10keV, $5x10^{15}$ $cm^{-2}$), respectively. The annealing process for dopant activation was performed by RTA (rapid thermal annealing) in an $N_2$ ambient with 2 steps. The step 1 is 650°C for 60 sec and step 2 is 700°C for spike. A physical thickness 8-9 nm $HfO_2$ as gate dielectric by Atomic Layer Chemical Vapor Deposition (ALD) and 120nm TiN as metal gate by Sputtering were deposited. In order to improve the interface layer between Si substrate and $HfO_2$, the annealing with 550°C 30 sec before PVD was performed. The TiN and $HfO_2$ were defined by dry etching to accomplish metal gate at last process for TFET and gFET. After the gate stack definition, a physical thickness ~30 nm SiOx layer was deposited by Plasma-Enhance Chemical Vapor Deposition (PECVD) and spacer formation. A thickness 10 nm Ni layer by sputtering system was deposited, and the annealing process for forming Ni silicide by RTA in a $N_2$ ambient at 250°C for 30 sec, followed by 30 sec at 500°C to accomplish dopant segregated (DS) process (Fig. 1) [9][12]. Both gFET and TFET are fabricated together with the same process for comparison in performance.

## 3. Results and discussion

For p-gFET, the implantation region of source would extend to below of gate region which is different from p-TFET (Fig. 2). The carrier transportation mechanism is BTBT current and the energy band diagrams show that tunneling region of p-gFET and p-TFET is in vertical and lateral direction, respectively. Therefore, the current of p-TFET is not influenced by gate length, and the current of p-gFET would be increased with the increment of gate to S/D overlap region [1-6]. The TEMs of the devices show the slightly increased interfacial layer (IL) and physical thickness of $HfO_2$ with DS process (500°C 30 sec) as compare to that of without DS process (Fig. 3). According the measured C-V characteristics, the dielectric constants of $HfO_2$ are 19.6 and 19.7 for with and without DS process, respectively. This indicates the 500°C 30 sec of DS process may not significantly degrade the quality of the HK layer. Besides, the DS process may improve the interface between HK and semiconductor by observing $D_{it}$ (Fig. 4). The extracted $D_{it}$ is calculated by high-low frequency C-V method, and the value at midgap is improved from $2x10^{11}$ to $6x10^{10}$ $cm^{-2}eV^{-1}$ with DS process. The main purpose of the DS process is lower parasitic resistance and increased dopant concentration to obtain steep junction profile. The I-V of $n^+/p$ junction shows improved ideal factor and higher current at high voltage in forward bias region, and lower current in reverse bias region (Fig. 5). Therefore, the DS process for S/D engineering was used in this study for excellent gFET and TEFT fabrication process (Fig. 1). The transfer characteristics $I_DV_G$ of gFET and TFET show more than 5 orders of ON/OFF ratio (Fig. 6), and minimum subthreshold swing (SS) as BTBT boost are 75 and 68 mV/dec, respectively (Fig. 6 & 7). The output characteristics $I_DV_D$ of gFET shows as high as 14 μA/μm with $|V_{GS}-V_{BTBT}|$=3V and $|V_{DS}|$=3V, and it is about 25 time higher than that of conventional TFET (Fig. 8). The reason of significant enhancement is due to larger area of BTBT region in vertical direction for gFET as compare to in lateral direction for TFET (Fig. 1). The leakage current is kept with similar for both gFET and TFET ~ $10^{-12}$ A/μm (Fig. 6), and it indicates the well control in dopant profile of $n^+$ region with DS process for both kind of devices. The gFET with vertical BTBT mechanism is valid benefit for driving current enhancement of TFET without sacrificing the leakage current and subthreshold swing for CMOS scaling down in the future generation.

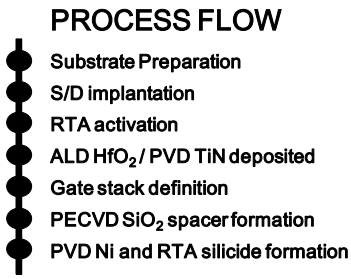
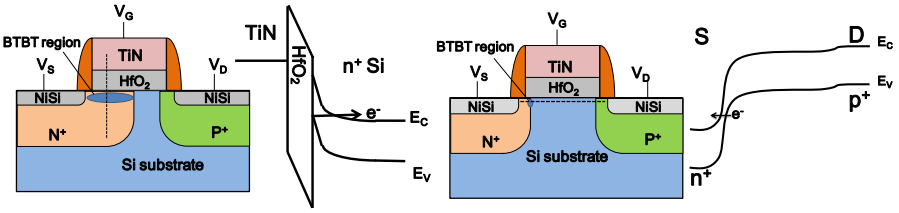
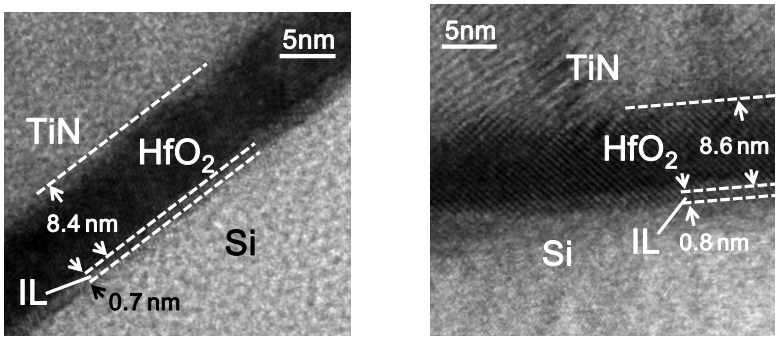



Fig. 1. The process flow of the gFET and conventional TFET with DS process. Both gFET and TFET are fabricated together with the same process for comparison in performance.




(a) (b)

Fig. 2. The schematic diagram of (a) p-type gFET and (b) conventional p-type TFET. For p-gFET, the implantation region of source would extend to below of gate region which is different from p-TFET. The energy band diagrams show that tunneling region of p-gFET and p-TFET is in vertical and lateral direction, respectively.




(a) (b)

Fig. 3. The cross-section HR-TEM of HKMG stacks (a) without DS process and (b) with DS process. The TEMs of the devices show the slightly increased interfacial layer and physical thickness of $HfO_2$ with DS process (500°C 30 sec) as compare to that of without DS process

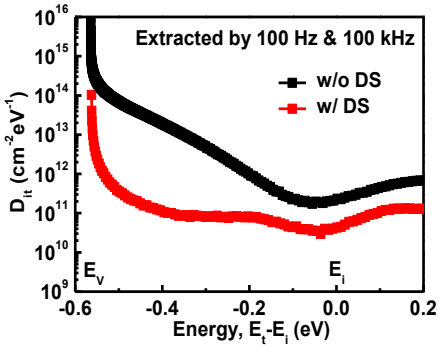



Fig. 4. The extracted $D_{it}$ (interface trap density) are calculated by high-low frequency C-V method, and the midgap value is improved from $2x10^{11}$ to $6x10^{10}$ $cm^{-2}eV^{-1}$ with DS process.

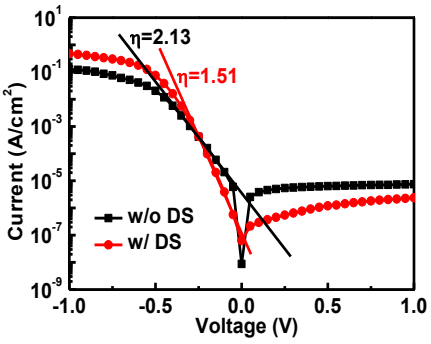



Fig. 5. The I-V of n+/p junction shows improved ideal factor and higher current at high voltage in forward bias region, and lower current in reverse bias region.

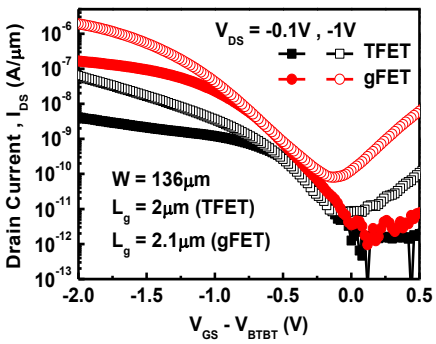



Fig. 6. The transfer characteristics $I_DV_G$ of gFET and TFET show more than 5 orders of ON/OFF ratio with similar leakage current.

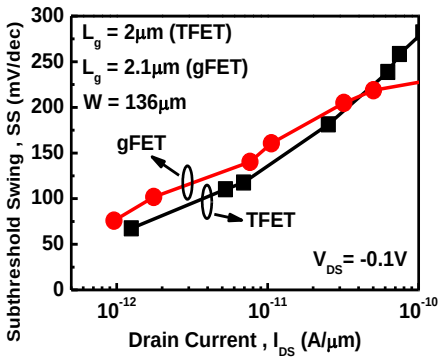



Fig. 7. The subthreshold swing (SS) vs. drain current. The minimum SS as BTBT boost are 75 and 68 mV/dec, respectively.

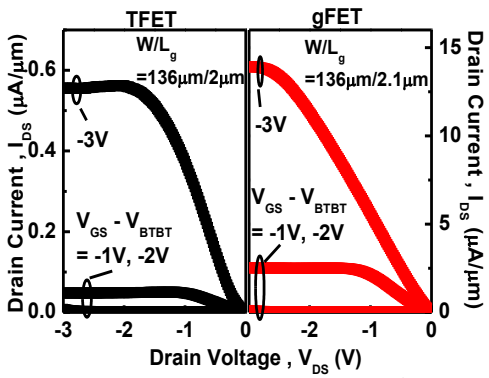



Fig. 8. The output characteristics $I_DV_D$ of gFET shows as high as 14 μA/μm with $|V_{GS}-V_{BTBT}|$=3V and $|V_{DS}|$=3V, and it is about 25 time higher than that of conventional TFET.

## 4. Conclusion

A high driving current of green transistors with DS process on bulk Si were successfully fabricated and developed. The gFET with vertical BTBT mechanism is valid benefit for ~ 25x ON current enhancement than that of TFET without sacrificing the leakage current and subthreshold swing for CMOS scaling down in future generation. The promising gFET with SOI free can be compatible with current process and avoid the issues of cost and thermal dissipation.

## 5. Acknowledgements

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