Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp86-87

PS-3-11

Wire-Orientation Dependence in Device Performances of Si and InAs Nanowire MOSFETs under Ballistic Transport

Kenta Shimoida[1], Yoshihiro Yamada[1], Hideaki Tsuchiya[1,2], and Matsuto Ogawa[1]

[1]Kobe University, Dept. of Electrical and Electronic Eng., 1-1, Rokko-dai, Nada-ku, Kobe 657-8501, Japan
[2]JST CREST, Chiyoda, Tokyo 102-0075, Japan
Phone & Fax (common): +81-78-803-6082 E-mail: 122t221t@stu.kobe-u.ac.jp

1. Introduction

Si nanowire MOSFETs (Si NWFETs) with gate-all-around (GAA) configuration have attracted much attention as a candidate of high performance and low power consumption VLSI devices. On the other hand, III-V semiconductors with high electron mobility are regarded as a post-Si channel material, and actually the high performance of InGaAs MOSFETs with high-k gate dielectrics has been demonstrated. Therefore, NWFETs incorporated with III-V channels are also expected to be a candidate for the future VLSI technology. In this paper, we study drive currents and consumption powers of Si and InAs NWFETs by using a ballistic FET model coupled with tight-binding (TB) band structure calculation, and then demonstrate the advantages of InAs NWFETs over the Si NWFETs.

2. Device Structure

We simulated square-shaped NWs grown in three different crystal orientations of <100>, <110> and <111>. The conduction band structures computed for the InAs NWs and the Si NWs are shown in Figs. 1(a)-(c) and (d)-(f), respectively. We employed the Jancu's and Boykin's parameters for the InAs NW and Si NW TB calculations, respectively. Here, the present InAs NWs have band gaps of ~1 eV or more, which allows us to neglect band-to-band tunneling leakage current at an off-state bias. First, the electron effective masses of the InAs NWs are found to be larger than the InAs bulk value ($0.023\,m_0$) [1,2], which is due to the non-parabolicity of the Γ valley. On the other hand, the <100>- and <110>-oriented Si NWs have conduction band minimum at the Γ point due to the k-space projection of the bulk six ellipsoidal bands [3,4], while the <111>-orientation has it at off-Γ point. As reported in [3-5], the <110>-oriented Si NWs have transport mass smaller than the bulk m_t ($= 0.19\,m_0$), while the other two orientations have larger transport masses than the bulk m_t, because of the Si anisotropic conduction band in the momentum-space.

3. Electrical Characteristics

Fig. 2 shows (a) the simulated GAA NWFETs and (b) the top-of-the-barrier (ToB) FET model [6] used to calculate the electrical characteristics in the ballistic limit, where any scattering mechanisms and tunneling effects at the off-state bias are neglected. Fig. 3 shows the I_D-V_G characteristics computed for EOT = (a) 3 nm, (b) 0.5 nm and (c) 0.25 nm. First, we notice that the performance dependence on the wire-orientation is not significant in the InAs NWFETs, compared to the Si NWFETs. This is due to the fact that the InAs NWs have effective masses nearly independent of the wire-orientation as indicated in Fig. 1, which is owing to an isotropic nature of the Γ valley. This may give us flexibility in layout design of integrated circuits. Next, it is found that the InAs NWFETs exhibit higher drain current than the Si NWFETs for EOT = 3 nm, as expected. However, as EOT reduces less than 0.5 nm, the drain current of the InAs NWFETs becomes comparable to or even smaller than the Si NWFETs, for the <100>- and <110>-orientations. To explore the cause, we plotted the channel charge densities and the averaged electron velocities as a function of gate voltage as shown in Fig. 4, where EOT = (a) 3 nm and (b) 0.25 nm. We can confirm that the averaged velocities are larger in the InAs NWFETs identically for both EOTs. On the other hand, the InAs NWFETs have smaller charge density than the Si NWFETs for both EOTs, but a further remarkable reduction is observed in the case of EOT = 0.25 nm. This is due to a smaller quantum capacitance (C_Q) of InAs NW channels caused by the smaller density-of-states [2]. Actually, Fig. 5 shows the computed C_Q's as a function of gate voltage, which indicates that the InAs NWFETs with EOT = 0.25 nm have significantly-smaller C_Q's than the oxide capacitance, C_{ox}. As a result, the total gate capacitance becomes approximately equal to C_Q, and the channel charge substantially decreases. The above results mean that the lower drain current in the InAs NWFETs with EOT < 0.5 nm is primarily due to the gate capacitance reduction owing to the smaller C_Q.

In the meantime, the quantum capacitance (QC) operation requires a much smaller charge density for switching a device as shown in Fig. 4, and hence reduction in the power-delay-product (PDP) is expected [2]. Fig. 6 shows the computed PDP densities as a function of ON-current, which demonstrates that a lower power switching is indeed anticipated in InAs NWFETs even under the QC limit (EOT < 0.5 nm), although its advantage becomes less significant.

4. Conclusions

By using the atomistic ballistic simulation, we have demonstrated that the InAs NWFETs have the advantage in terms of lower power operation over the Si counterpart, and furthermore provide greater flexibility in layout design of practical integrated circuits.

Acknowledgements This research was supported by a Grant-in-Aid for Scientific Research from the Japan Society for the Promotion of Science (JSPS), and the Japan Science and Technology Agency (JST)/CREST.

References [1] K. Alam et al., *IEEE-TED* **57** (2010) 2880. [2] N. Takiguchi et al., *IEEE-TED* **59** (2012) 206. [3] N. Neophytou et al., *IEEE-TED* **55** (2008) 1286. [4] H. Tsuchiya et al., *IEEE-TED* **57** (2010) 406. [5] Y. Yamada et al., *JAP* **111** (2012) 063720. [6] A. Rahman et al., *IEEE-TED* **50** (2003) 1853.

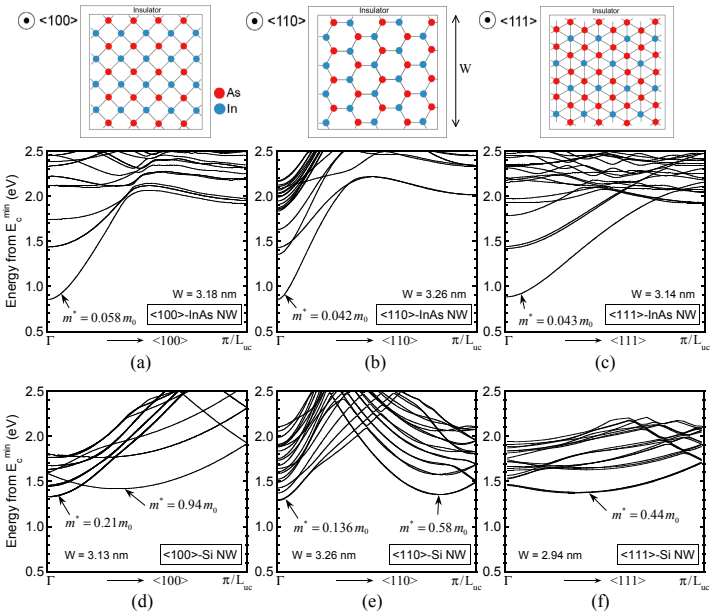

Fig. 1 Conduction band structures computed for InAs NWs ((a)-(c)) and Si NWs ((d)-(f)) with <100>-, <110>- and <111>-orientations, where the cross section is about 3 nm for all NWs. The origin of the vertical axis, i.e., $E = 0$, corresponds to the Fermi level. Some effective masses are also indicated.

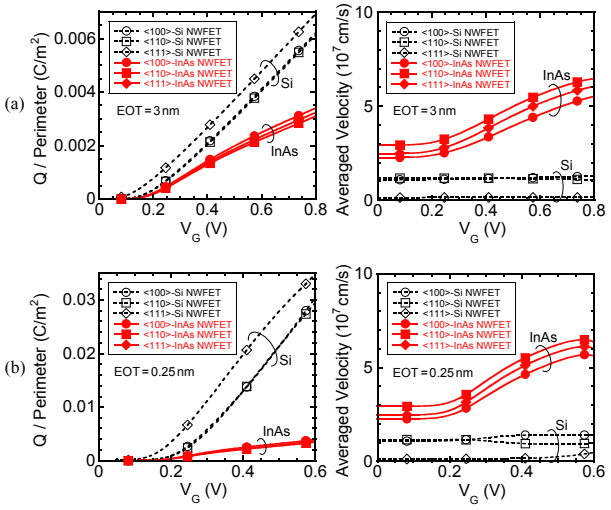

Fig. 4 (Left column) Computed channel charge densities normalized by the perimeter of NWs and (right column) averaged electron velocities as a function of gate voltage, where EOT = (a) 3 nm and (b) 0.25 nm.

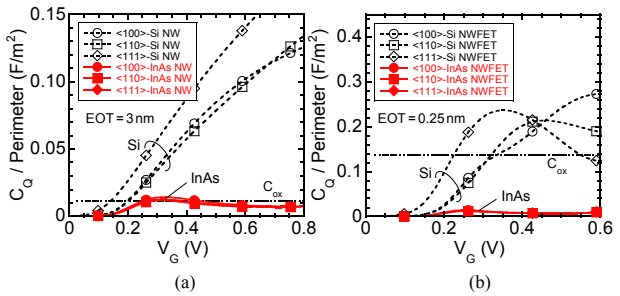

Fig. 5 Computed quantum capacitance values as a function of gate voltage corresponding to the I_D - V_G curves in Fig. 3 (a) and (c). The vertical axis is normalized by the perimeter of NWs. The horizontal dashed lines represent the oxide capacitance values, C_{ox}.

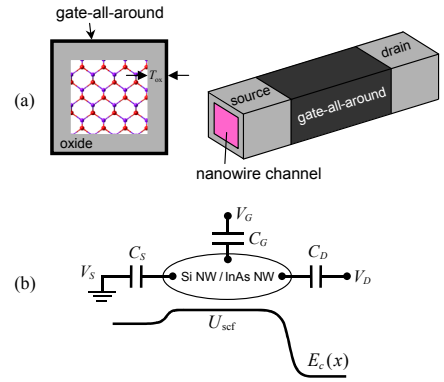

Fig. 2 (a) Simulated GAA-NWFETs and (b) ToB-FET model used to calculate electrical characteristics.

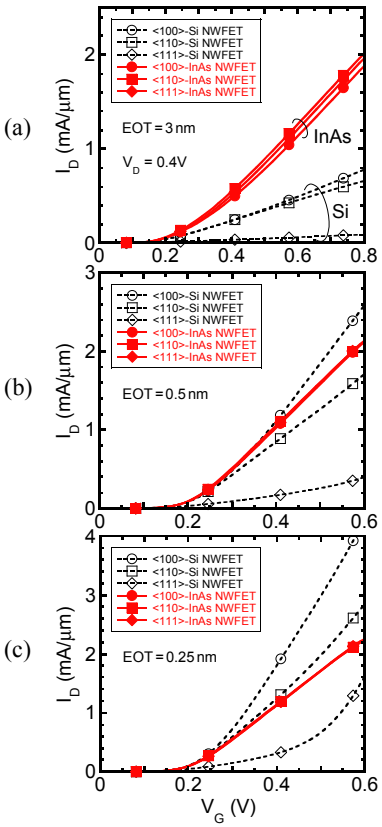

Fig. 3 I_D - V_G characteristics computed for EOT = (a) 3 nm, (b) 0.5 nm and (c) 0.25 nm. The vertical axis denotes drain current density normalized by the perimeter of NWs. V_D = 0.4 V. I_{OFF} = 0.01 μA/μm.

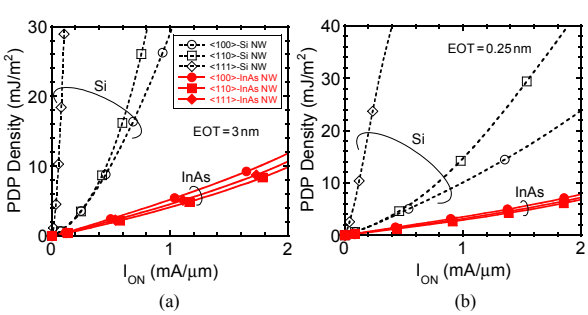

Fig. 6 Computed PDP densities as a function of ON-current for EOT = (a) 3 nm and (b) 0.25 nm, where V_D = 0.4 V. The vertical axis is divided by the in-plane device area, and L_{ch} = 10 nm.