Monte Carlo Study on the Role of High Channel Doping in Junctionless Transistors

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1. Introduction

Recently, a junctionless (JL) transistor with no pn junctions has been proposed [1,2]. In this device, doping type and concentration in the channel are identical to those in the source and drain, and hence there are no junctions and no doping concentration gradients between source and channel or drain and channel. This simple structure requires no costly ultrafast annealing techniques and thus allows us to fabricate ultrashort-channel MOSFETs [1]. Furthermore, JL transistors have a number of advantages, such as less sensitivity to the channel-gate oxide interface, carrier transport with bulk mobility, which is typically higher than the inversion layer mobility, and better speed performance.

On the other hand, impurity scattering in the channel may decrease the carrier mobility and degrade the device performance. In this paper, we investigate the role of the high channel doping in the device performance of JL transistors based on a Monte Carlo (MC) simulation.

2. Device Structure

The key technique to obtaining a properly working JL transistor is the formation of an ultrathin or ultranarrow channel with a proper gate work function so that the channel region can be fully depleted when the device is turned off. Meanwhile, the channel needs to be heavily doped to obtain a sufficiently large drive current at ON-state [1,2]. Therefore, we employed here an ultrathin-body double-gate (DG) MOSFET shown in Fig. 1. To compare with the performances of conventional DG devices, the doping concentration in the source and drain is taken to be highly sufficient, \( N_D = 1 \times 10^{20} \text{ cm}^{-3} \). For simulations of JL transistors, the doping concentration in the channel \( N_{ch} \) is set at the same value as the above \( N_D \), while it is assumed to be zero for the conventional devices. The electrical characteristics were computed by using a MC device simulation [3,4], where any quantum effects were disregarded. We considered phonon and impurity scatterings, while roughness scattering was ignored to examine the roles of the gate electrostatic controllability and the impurity scattering in the channel of JL transistors.

3. Electrical Characteristics

First, Fig. 2 shows the \( I_D - V_G \) characteristics, where (a) and (b) correspond to \( T_{Si} = 10 \) and 5 nm, respectively. Here, the channel length \( L_{ch} \) was provided by following an empirical rule of \( L_{ch} = 4 \times T_{Si} \). First of all, the conventional DG devices are found to work well for both \( T_{Si} \)'s. On the other hand, the JL transistor with \( T_{Si} = 10 \text{ nm} \) indicates a lack of switching behavior, which means that it is a simple \( n' - n - n' \) resistor. However, as the channel thickness decreases to 5 nm, it exhibits a well-behaved transistor operation as shown in Fig. 2(b), which is owing to the enhanced gate electrostatics. These results reconfirm that the channel thickness must to be smaller than the depletion layer width to make JL transistors work properly [1,2,3].

Next, Fig. 3 shows the \( I_D \) versus gate overdrive characteristics for the \( T_{Si} = 5 \text{ nm} \) device. It is found that the JL transistor exhibits a large ON-current and good turn-on characteristics, quite comparable to those of the conventional one. The result is consistent with the experimental measurement [1]. This is a good news for JL transistors, because it suggests that high channel doping does not degrade the drive current seriously. One of the reasons is that the Coulomb interaction with ionized impurities scatters electrons mostly forward [3,4], and thus electrons are less likely to be returned to the source even if they are scattered by impurities within the channel (See the dashed-dotted line, which indicates that the isotropic impurity scattering model significantly decreases \( I_D \)). Another reason is that source parasitic resistance, \( R_S \), is smaller in the JL MOS transistor at ON-state as shown in Fig. 4(a). Both the forward scattering nature of ionized impurities and the smaller \( R_S \) contribute to obtain the averaged electron velocity comparable to that of the conventional MOS transistor as shown in Fig. 4(b) [3].

Here, we should point out that high-energy electrons accelerated by a high electric field in such an ultrashort-channel device are more likely to be scattered forward than low-energy electrons. To demonstrate this, we also simulated longer channel devices with \( L_{ch} = 100 \text{ nm} \), and as shown in Fig. 6(a), a lower electric field actually prevails within the channel for \( V_G - V_A = 0.1 \text{ V} \). As a result, the impurity scattering becomes isotropic to significantly reduce the averaged velocity down to the same level as the isotropic model as shown in Fig. 6(b). Thus \( I_D \) distinctly decreases at the small gate bias condition as shown in Fig. 5. On the other hand, as \( V_G \) increases, the \( I_D \) approaches to the conventional one due to the contributions from the forward scattering nature of ionized impurities and the smaller \( R_S \) in the JL transistor as seen in Figs. 6(d)-(f). The above results mean that the impurity scattering has a smaller negative influence on the ON-current as compared to the mobility degradation observed in a low electric field regime.

4. Conclusions

We have demonstrated that the high channel doping does not degrade the drive current of JL transistors seriously, because of the forward scattering nature of ionized impurities, and the smaller parasitic resistance in JL transistors.

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Fig. 1 Device structure. The doping concentration in the source and drain, \( N_D \), is \( 1 \times 10^{20} \text{ cm}^{-3} \). For simulations of JL transistors, the doping concentration in the channel, \( N_{ch} \), is set at the same value as the above \( N_D \), while it is assumed to be zero, that is, the channel is intrinsic, for the conventional devices. A p' (n') polysilicon gate is used for JL (conventional) transistors, where we considered n-channel MOSFETs. The channel thicknesses \( T_{Si} \) are given as 10 and 5 nm, to examine the roles of miniaturization of the channel cross section. The channel length \( L_{ch} \) is provided by following an empirical rule of \( L_{ch} = 4 \times T_{Si} \), which is often used as a guideline to suppress short-channel effects.

Fig. 2 \( I_D-V_G \) characteristics computed for both JL and conventional MOS transistors, where (a) \( T_{Si} = 10 \text{ nm} \) and \( L_{ch} = 40 \text{ nm} \) and (b) \( T_{Si} = 5 \text{ nm} \) and \( L_{ch} = 20 \text{ nm} \). The drain voltage \( V_D \) is set at 0.5 V. The right panels indicate the logarithmic plot of the drain current. From (b), current slopes at the minimum gate voltage are qualitatively the same behavior as the experimental measurement in [1]. Also note that \( I_D \) reduction with the isotropic impurity scattering model is more significant, compared to Fig. 3. This is simply due to the longer \( L_{ch} \).

Fig. 3 \( I_D \) versus gate overdrive characteristics of JL and conventional transistors with \( L_{ch} = 20 \text{ nm} \), where \( T_{Si} = 5 \text{ nm} \) and the threshold voltage \( V_{th} \) was defined as a gate voltage corresponding to \( I_D = 0.03 \text{ mA/um} \). The dashed-dotted line represents the result calculated by assuming isotropic impurity scattering where electrons are scattered equally forward and backward due to ionized donors. The right panels indicate the logarithmic plot of the drain current.

Fig. 4 (a) Potential energy, (b) averaged electron velocity and (c) sheet electron density profiles computed at \( V_G - V_{th} = 0.4 \text{ V} \). \( L_{ch} = 20 \text{ nm} \) and the channel region extends from \( y = 30 \) to 50 nm. \( T_{Si} = 5 \text{ nm} \) and \( V_D = 0.5 \text{ V} \). Note that the magnitude relation of the drain currents is primarily determined by the electron velocity, because the channel electron densities are nearly identical among the three results as shown in (c).

Fig. 5 \( I_D \) versus gate overdrive characteristics of JL and conventional transistors with \( L_{ch} = 100 \text{ nm} \), where \( T_{Si} = 5 \text{ nm} \) and \( V_D \) was defined in the same manner as Fig. 3. The present results represent qualitatively the same behavior as the experimental measurement in [1]. Also note that \( I_D \) reduction with the isotropic impurity scattering model is more significant, compared to Fig. 3. This is simply due to the longer \( L_{ch} \).

Fig. 6 Potential energy, averaged electron velocity and sheet electron density profiles computed at \( V_G - V_{th} = 0.1 \text{ V} \) (a)-(c) and 0.4 V ([d]-[f]). \( L_{ch} = 100 \text{ nm} \) and the channel region extends from \( y = 30 \) to 130 nm. \( T_{Si} = 5 \text{ nm} \) and \( V_D = 0.5 \text{ V} \).