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Extraction of Carrier Concentration and Mobility of Heavily Doped Poly-Si Nanowires with Junctionless (JL) Transistor Structures

Zer-Ming Lin[a], Horng-Chih Lin[a,b,*], and Tiao-Yuan Huang[a]
[a] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University,
No. 1001, Ta Hsueh Rd., Hsinchu, Taiwan 300, R.O.C.
[b]National Nano Device Laboratories, No. 26, Prosperity Rd. I, Science-Based Industrial Park, Hsinchu, Taiwan 30078, R.O.C.
[*]Phone: +886-3-571-2121 ext. 54193, Fax: +886-3-572-4361, E-mail: hclin@faculty.nctu.edu.tw

1. INTRODUCTION

Recently, transistors with junctionless (JL) scheme have been demonstrated for logic [1] and memory device applications [2]. Such a scheme is also very promising for construction of 3D poly-Si-based devices [3] and circuits since it can greatly simplify the processing by eliminating the implant steps. However, few approaches are available for probing some of the important characteristics, such as carrier concentration and mobility, in the tiny but heavily doped nanowire (NW) channels. In this study, we propose a very simple methodology which only involves the measurements of I-V characteristics of a JL device built with poly-Si NW channels and gate-all-around (GAA) configuration.

2. DEVICE STRUCTURE AND CHARACTERISTICS

Figs. 1(a) and (b) show the 3D schematic structure and top view, respectively, of the GAA JL poly-Si NW devices characterized in this study. As shown in Fig. 1(a), the GAA JL TFT features two embedded heavily phosphorous-doped poly-Si NWs serving as the conduction channel. Details of the process flow can be seen in our previous work [3]. Note that the *in situ* doped n^+ poly-Si NW structure was prepared with an LPCVD process. Two splits of devices with different cross-sectional NW dimensions were characterized. The first group, denoted as "Device A", has a larger cross-sectional area of 70×27 nm^2, as can be seen from the cross-sectional scanning electron microscopic (SEM) image shown in Fig. 2. The other group features a NW with cross-sectional area of around 23×12 nm^2. Its cross-sectional SEM image can be found in our previous work [3].

Fig. 3 shows the great impact of the NW dimensions on the I_D-V_G characteristics of the devices. By reducing the cross-sectional area of the NW channels, good switching ability and high on/off current ratio can be achieved. On the other hand, although Device A cannot be effectively turned off because of its large cross-sectional area, its transfer characteristics can be cleverly utilized to extract the active doping concentration and mobility of the *in situ* phosphorous-doped poly-Si NWs with theoretical analysis and measurement procedure stated below.

3. EXTRACTION OF CARRIER CONCENTRATION AND MOBILITY

First, we detail the theoretical background of the methodology. Fig. 4 schematically shows the cross-sectional structural parameters of the device along line A-A' shown in Fig. 1(b). Owing to the rather thick structure and the heavy channel doping, the investigated Device A is partially depleted during the off-state operation and the depletion width, X_{depl}, is expected to be much smaller than either H or W. Therefore, 1D Poisson's Equation is suitable for calculating the electric potential. The analytical solution of electric potential and the necessary boundary conditions applied to the 1D Poisson's Equation are summarized in Table. I. With the analytical solution of electric potential, the maximum depletion width ($X_{depl,max}$) and the gate voltage ($V_{G,off}$) as $X_{depl,max}$ is reached can be evaluated. Expressions of the derived $X_{depl,max}$, $V_{G,off}$ as well as flat-band voltage (V_{FB}) are summarized in Table II. As V_G is smaller than $V_{G,off}$, $X_{depl,max}$ is reached and maintained. Meanwhile, the conduction current through the core neutral region is no longer affected by the applied V_G. Namely, the transfer characteristics of the JL transistors switch from "gated resistor" to "ungated resistor", as schematically shown in Fig. 5. As $X_{depl,max}$ is reached, the conduction area of the ungated resistor is equal to the cross-sectional area of NW minus the area of the depletion region. Table III summarizes the expression of the conduction area and the resistance of the device as operated in the "ungated resistor" regime. The above inference and prediction are confirmed with the I_D-V_G curves measured at V_D ranging from 0.25 to 1.25 V shown in Fig. 6(a) in which we can see that two distinct regions can be distinguished. Results of the transconductance (G_m) as a function of V_G are shown in Fig. 6(b). Since G_m is the differentiation of I_D to V_G, it suddenly drops to zero when the device is switched from gated- to ungated-resistor behavior. $V_{G,off}$ can thus be extracted in the figure as the V_G when G_m drops to zero, which is -9.1 V in this case. Moreover, V_{FB}, which is equal to 2.88V, can also be determined as the V_G corresponding to the G_m peaks in Fig. 6(b) [4]. With the value of $V_{G,off}$ and V_{FB} applied to Eqs. 6 and 7 (Table II), the active doping concentration (n) and fixed charges (Q_{fix}) can be evaluated and the results are $1.18\times10^{19}cm^{-3}$ and -3.25×10^{12} cm^{-2}, respectively. To extract mobility (μ), I_D in Fig. 6(a) measured at V_G=-10V is shown as a function of V_D in Fig. 7. It can be seen that the current is proportional to V_D and its slope, which is equal to 1/R, is 4.5×10^{-7} (Ω^{-1}). Based on the result and Eq. 9 (Table III), the mobility is determined to be 52.5 cm^2/V-sec. Finally, it is worthy to make some careful checks to confirm the accuracy of the extracted parameters. First, by applying the extracted carrier concentration to Eq. 5, the estimated $X_{depl,max}$ is around 11nm, which is indeed smaller than H(=27nm) and W(=70nm). Second, by applying the extracted parameters to a TCAD simulation tool, the electric potential across the middle of the NW along the y-direction (see Fig. 4) under various V_G conditions can be calculated and the results are shown in Fig. 8. It can be seen that the electric potential is almost flat at V_G=2.88V, confirming the feature of flat-band condition. This result supports the accuracy of the methodology in extracting V_{FB}.

4. CONCLUSION

A very clever and simple procedure for extracting the carrier concentration, mobility, and interface fixed charge density of *in situ* phosphorous-doped poly-Si NWs is conceived and demonstrated. The principle of the methodology mainly relies on the switching of operation of a GAA JL device from gated to ungated mode. The scheme can be readily implemented in the manufacturing and characterization of future poly-Si based 3-D devices.

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References

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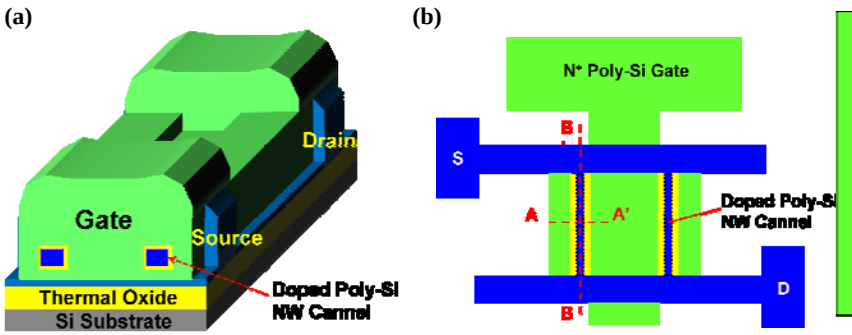

Fig. 1 (a) Stereo and (b) top views of the fabricated GAA JL poly-Si NW transistors.

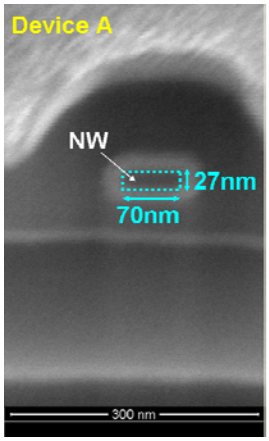

Fig. 2 Cross-sectional SEM image of Device A along line AA' shown in Fig. 1(b).

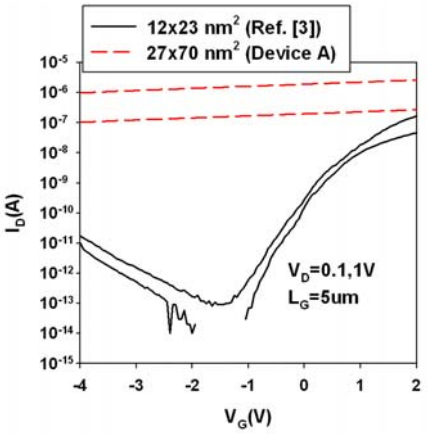

Fig. 3 Comparisons of I_D-V_G characteristics for two devices featuring NWs with different cross-sectional area.

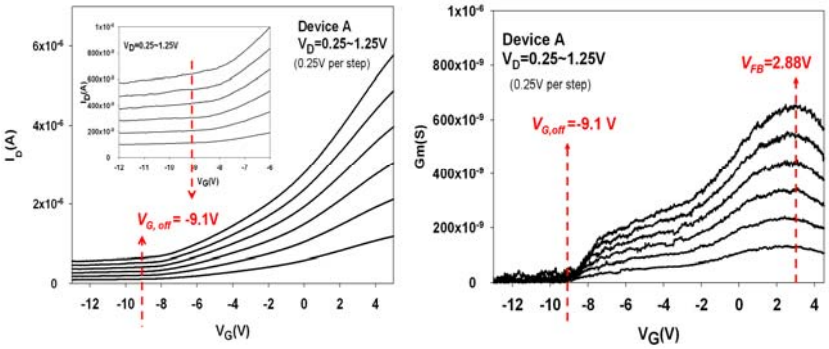

Fig. 6 (a) Transfer characteristics of Device A as a function of V_D. (b) Gm versus V_G measured at various V_D.

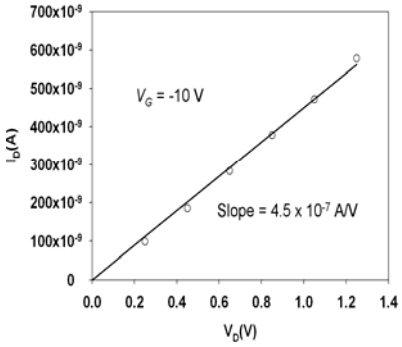

Fig. 7 I_D extracted from Fig. 6(a) at V_G=-10V as a function of V_D.

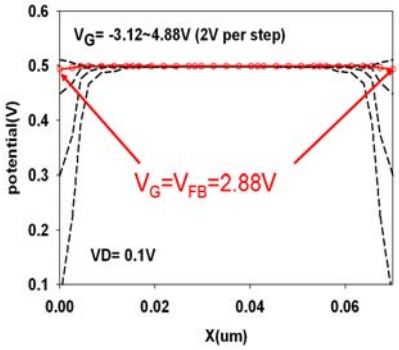

Fig. 8 Simulated electric potential distributions in the middle of the NW along y-axis at V_D=0.1V and various V_G.

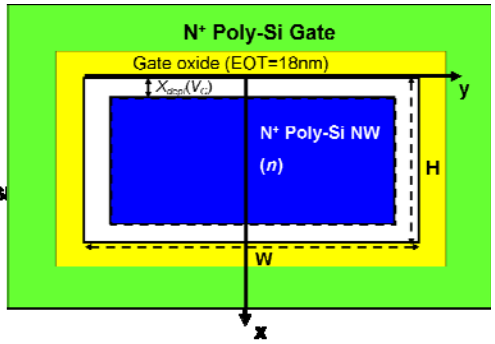

Fig. 4 Schematic illustration of the cross-sectional structure of the GAA JL transistor as $V_G < V_{FB}$ along line AA' shown in Fig. 1(b). EOT is effective oxide thickness, which is equal to 18nm in this case. X_{dep} is the depth of depletion region and n is the active doping concentration.

Table. I 1D Poisson equation and the analytical solution of electric potential

1D Poisson's Eq.
$\frac{d^2\Phi(x)}{dx^2}=\frac{-qn}{\varepsilon_{si}}$, (1)
Two Boundary Conditions
$E(x=X_{dep})=0$ (2)
$\Phi(x=X_{dep})=0$ (3)
Solution of Electric Potential
$\Phi(x)=\frac{qnX_{dep}}{\varepsilon_{si}}x-\frac{qn(x^2+X_{dep}^2)}{2\varepsilon_{si}}, 0<x<X_{dep}$. (4)

Table. II Summary of the analytical expression of $X_{dep,max}$, $V_{G,off}$ and V_{FB}. $X_{dep,max}$ is the maximum depth of depletion region. $V_{G,off}$ is the applied gate voltage as $X_{dep,max}$ is reached

$X_{depl,max}=\sqrt{2\varepsilon_{si}[E_g/2+kT/q\ln(n/n_i)]/qn}$. (5)
$V_{G,off}=V_{FB}-\frac{qnX_{depl,max}}{C_{ox}}-(\frac{E_g}{2})+\frac{kT}{q}\ln(\frac{n}{n_i})$. (6)
$V_{FB}=\frac{E_g}{2}-\frac{kT}{q}\ln(\frac{n}{n_i})-\frac{Q_{fix}}{C_{ox}}$. (7)

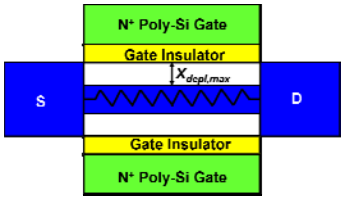

Fig. 5 Schematic illustration of the cross-sectional structure of the GAA JL transistor as $V_G < V_{G,off}$ along line BB' shown in Fig. 1(b).

Table. III Analytical expression of conduction area and current of ungated resistor.

Conduction Area
$H\times W-2(H+W)X_{depl,max}+4X_{depl,max}^2$. (8)
Resistance of Ungated Resistor
$R=V_D/I_D$
$=L/nq\mu(H\times W-2(H+W)X_{depl,max}+4X_{depl,max}^2)$. (9)