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Off-Current Fluctuations in 10-nm Trigate MOSFETs – Impact of the Channel Geometry

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1. Introduction

Minimizing random fluctuations of the device performance due to process variations or other sources like random discrete dopants (RDD) or random telegraph noise (RTN) is one of the major challenges for CMOS scaling [1-3]. To minimize fluctuations due to RDD, MOSFET concepts with undoped channels are suggested. Among them, the trigate SOI MOSFET is one of the most promising candidates for CMOS generations with gate lengths below 20nm. Since the channel is undoped, the electrostatic integrity of a trigate MOSFET strongly depends on the channel geometry, i.e. on the width w_{Si}, height t_{Si} and length L_G of the silicon body (Fig. 1). Random deviations of these parameters from their nominal values will lead to severe fluctuations of parameters like threshold voltage, on-current I_{on}, and off-current I_{off}. Because of the small dimensions, such fluctuations can strongly be enhanced by quantum effects [4]. Moreover, the presence of a single charged impurity in the active device region can significantly alter the electrical performance [2, 5].

In this simulation study, we investigate the sensitivity of various trigate (TG) and single-gate (SG) SOI designs with L_G = 10nm to variations of the channel geometry and to single charged impurities at the channel/oxide interfaces. Special emphasis is paid to the effects of quantum confinement. We focus our discussion to I_{off} showing very strong fluctuation effects in the investigated structures.

2. Simulation Methodology

Figure 1 shows the considered TG MOSFET structure featuring a gate dielectric with an equivalent oxide thickness of 0.6nm and a 20nm thick buried oxide (BOX). The simulations are performed using ATLAS applying the drift-diffusion model with a modified velocity-field characteristics [6]. The effects of quantum confinement have been calculated by analytical models [4] or self-consistent 2D Schrödinger-Poisson simulations [7]. A supply voltage of 0.8V is assumed.

From the simulated transfer characteristics of devices with various combinations of w_{Si} and t_{Si}, the design space for both parameters, the green area in Fig. 2, has been extracted. The upper boundary (blue solid line with symbols) sets the limit for (t_{Si}, w_{Si}) combinations necessary to meet the target values for I_{on} (1820µA/µm) and I_{off} (110nA/µm) for high-performance logic applications. The lower boundary (red solid curve) is defined by quantum effects. In designs with (w_{Si}, t_{Si}) left from or below the red line, quantum effects are so strong that combined variations of w_{Si} and t_{Si} by only one atomic layer lead to I_{off} changes by more than a factor of 2 in a long channel device. The black dash-dotted lines denote the upper limits for t_{Si} and w_{Si} for the ideal 2D cases single-gate (SG) SOI MOSFET ($w_{Si} \to \infty$) and double-gate (DG) MOSFET ($t_{Si} \to \infty$).

3. Geometry fluctuations

Three different trigate designs (TG1…TG3) from the green area in Fig. 2, together with a SG and a DG structure with comparable I_{on}/I_{off} behavior (Table I) have been chosen to study the sensitivity of I_{off} to geometry fluctuations. The results are summarized in Fig. 3. In Fig. 3(a) the separate sensitivities to variations of t_{Si}, w_{Si} and L_G are shown. The smaller t_{Si} (w_{Si}) of a structure is, the higher is the I_{off}-sensitivity to variations of this dimension with an increasing impact of quantum effects. The sensitivity to L_G variations is similar in all structures due to the comparable immunity against short-channel effects. Figure 3(b) shows the combined effect of geometry fluctuations on I_{off}. Two cases are considered: all dimensions can vary (i) by one atomic layer (1.36Å) or (ii) by 10% of their nominal values. Case (i) can be considered as the lower limit for the geometry fluctuations in general. In this case the SG MOSFET shows the largest I_{off}-variation (factor 3), whereas the DG-like TG3 exhibits the most stable I_{off} (factor 1.9). In the more realistic case (ii), I_{off} varies in general by more than one order of magnitude. Here the SG-like TG1 has the smallest I_{off}-variation (factor 25), while TG2 shows the strongest one (factor 39). From the classical results for case (ii) (dashed red curve in Fig 3b) it turns out that I_{off}-fluctuations tend to increase in the direction toward DG-like designs. Quantum effects, on the other hand, are strongest for $t_{Si} \sim w_{Si}$ (compare red curve in Fig. 2) making the TG2 design most sensitive to geometry fluctuations in case (ii). However, this result does not mean that TG2 would be a bad choice. It rather means that the final choice of the TG design should depend on the actual process induced fluctuations of the channel geometry.

4. Charged impurities

The presence of a single charged impurity in the device can have various reasons. Acceptor like interface traps, for instance, are the main source of RTN which is a time dependent current fluctuation. Other possibilities are fixed oxide charges or single dopants originating from the unintentional background doping or the source/drain regions. Such charges can either be negative or positive.

As can be seen from Fig. 4, a single charged impurity can have a tremendous effect on the subthreshold currents in the SG and TG MOSFETs considered here. For the impurities, two locations at the channel/oxide interfaces have been considered: at the center of (i) the top gate oxide and (ii) the BOX. At these locations in the middle of the channel, the effect on the potential barrier between source and drain is exceptionally strong. A charge at the BOX interface, however, is the worst case, leading to off-current fluctuations by more than a factor of 70 in TG2 (with a positive charge). From Schrödinger-Poisson simulations it turns out that quantum effects tend to reduce the effect of a positive charge at the BOX by about 25%, while increasing the effect of a negative charge by a similar amount.

From Fig. 4(b) it can be seen that in all designs a charge at the BOX interface has a similar effect on the subthreshold current. The largest effect is observed in TG2 (factor 72), whereas TG3 (factor 42) is the least affected design. A charge at the top gate oxide, on the other hand, has the strongest effect in TG1 and in the SG MOSFET. As can be seen, the influence of such an impurity can successfully be suppressed when w_{Si} is reduced. Hence TG3 exhibits the smallest sensitivity. In other words, the closer an impurity is located to the gate electrode, the more effective the channel potential can be shielded from the influence of this charge. Thus, a more aggressively scaled channel cross-section (more than necessary for meeting the I_{on}/I_{off} requirements) would be beneficial for the robustness against charged impurities in general. Thinning the BOX could also be an option to increase the shielding effect by the backside substrate. The ultimate solution in this respect would be a gate-all-around structure with a very small silicon cross-section.

5. Conclusion

Our simulations have shown that both geometry fluctuations and single charged impurities can easily alter the off-currents of SG and TG SOI MOSFET designs that nominally meet the I_{on}/I_{off} requirements for L_G = 10nm by more than one order of magnitude. Regarding the robustness against geometry fluctuations, none of the investigated SG and TG structures can be preferred in general. For a given technology, however, the TG design can be optimized for minimum I_{off} fluctuations. To reduce the effect of single charged impurities on I_{off}, the channel cross-section should be scaled more aggressively than necessary for meeting the I_{on}/I_{off} requirements.

Acknowledgement

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References

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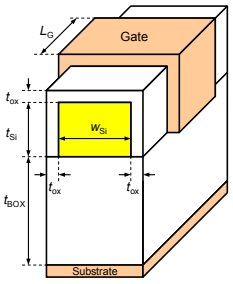

Fig. 1 Trigate MOSFET simulated in this work.

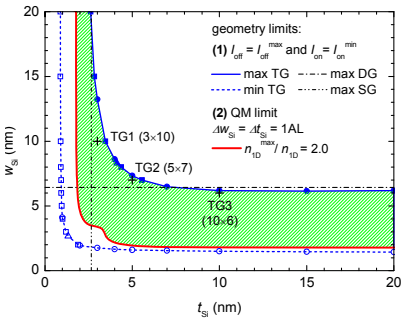

Fig. 2 Design space for the channel dimensions w_{Si} and t_{Si} (green area).

Table I Key parameters of chosen SG, TG and DG designs

	SG	TG1	TG2	TG3	DG
$t_{Si} \times w_{Si}$ (nm^2)	2.5 × ∞	3 × 10	5 × 7	10 × 6	∞ × 6
I_{off} (μA/μm)	0.11	0.11	0.11	0.11	0.11
I_{on} (μA/μm)	1909	1951	1876	1876	1957
DIBL (mV/V)	-176	-124	-144	-157	-182
S (mV/dec)	99.8	93.5	97.7	98.4	96.8

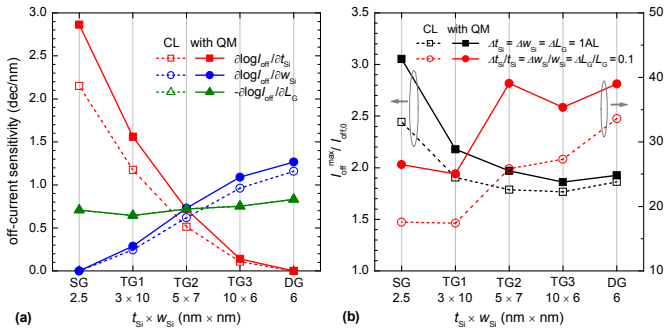

Fig. 3 (a) I_{off} sensitivities to variations of t_{Si}, w_{Si} and L_G. (b) Ratio between maximum and nominal I_{off} due to geometry variations by one atomic layer (black squares) and by 10% of the nominal values (red circles) with (full symbols) and without (open symbols) quantum effects.

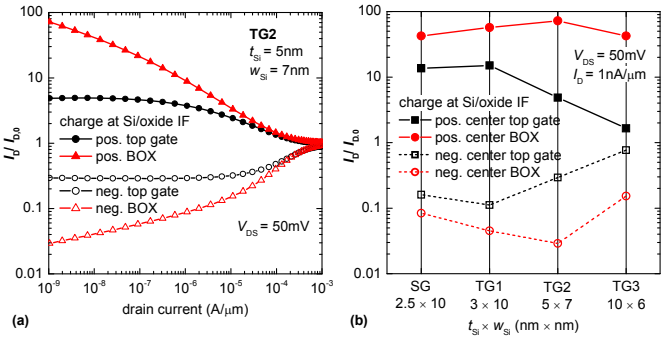

Fig. 4 Current fluctuations due to a single positive (full symbols) or negative (open symbols) charge at the channel/BOX (red) or the channel/top gate oxide (black) interface. (a) Ratio between altered and nominal drain current in TG2. (b) Comparison of chosen SG and TG designs.