Influence of Structural Parameters on Performance of Schottky Tunneling FET Electrical Characteristics and its Scalability

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1. Introduction

As the MOSFET scaling goes down to 10nm region, the supply voltage (V_{dd}) and the threshold voltage should be decreased accordingly[1] However, if the threshold voltage is scaled with large subthreshold swing (SS) due to the short channel effect, the current at the zero gate voltage $I_{\rm off}$ would increase. For this reason, devices with sharp subthreshold characteristics have been developed. The tunnel FET is one of the promising candidates to decreases SS. Schottky barrier tunneling FET (SBTFET)[2], which uses Schottky tunnel junction, has many advantages to ordinary PN junction tunnel FETs [3]: low parasitic resistance, better short channel effect (SCE) immunity and high controllability of output characteristics by the silicide material selection. In this work, device simulation has been performed to investigate the structural parameter influence on the electrical characteristics of SBTFETs. With the Schottky barrier height optimization, the SBTFET showed better performance than the conventional SOI-MOS-FET in 10nm region.

2. Simulation and Device Structure.

Silvaco TCAD tool ATLAS (ver.1.3.14.C) with the universal Schottky tunneling model [5] was used for this work. N-type silicon SOIMOS structure (Fig.1) was used in this simulation. Source-to-channel contact is the Schottky contact with various barrier height $\phi_{\rm B}$, while drain-to-channel contact is ohmic ($\phi_{\rm B}$ =0). The constant device parameters are the gate oxide thickness (0.3nm), SOI layer thickness (6nm), and BOX thickness (1000nm). The metal gate work function was set to be 4.8eV. The parameters such as $\phi_{\rm B}$, channel carrier concentration (*Na*), tunneling mass (*m**) were varied around default values ($\phi_{\rm B}$ =0.61eV, *Na*=2x10¹⁹ cm⁻³, *m**=0.08[6]). Through all *Na* value, this device is the fully depleted SOIMOS. The drain voltage is set to be 0.3V.

3. Result and Discussion

Figures 2 and 3 show the $I_{\rm D}$ - $V_{\rm G}$ and SS characteristics of SBTFET for various ϕ_B and Na for long channel ($L_{\rm G}$ =50nm). Id in SBTFET consists of the thermionic component $I_{\rm TH}$ and the tunneling component $I_{\rm TN}$. The characteristics only for $I_{\rm TH}$ are also shown in Fig.2, indicating that $I_{\rm TH}$ governs Id for low $V_{\rm G}$, while $I_{\rm TN}$ dominates high $V_{\rm G}$ region. It indicated that the SS minima are at the $V_{\rm G}$ area in which Id is governed by $I_{\rm TN}$. These figures also show that lower ϕ_B and larger Na lead to better subthreshold characteristics as a general trend. As an imaginary practice, m^* is modified as shown in Fig.4 and it was confirmed that the lighter tunneling mass would directly leada to sharper subthreshold characteristics as expected. Tunneling rate distribution map at source corner of the devices for ϕ_B :0.81eV (a), and 0.41(b) at V_G =0.45 and 0.55V are shown in Fig.5. For large ϕ_B , the distribution hardly changed with the increase in $V_{\rm G}$, while the obvious tunneling probability enhancement was observed for small ϕ_{B} . This may be due to the drastic enhancement of the tunneling probability for large numbers of electrons near the Fermi level in the source electrode for low $\phi_{\rm R}$. The potential distributions at the source corner for devices (Fig.6) with low Na (a) and high Na (b) indicate that increase in Na leads to the abruptness of the potential, resulting in smaller SS, especially for large $V_{\rm G}$ area. Comparison between the conventional SOIFET and SBTFET $(\phi_B: 0.61 \text{ eV})$ indicates that SS of the SBTFET is larger for large $L_{\rm G}$ but smaller for $L_{\rm G}$ below 10nm. The SS as a function of $L_{\rm G}$ is illustrated along with the $V_{\rm TH}$ roll-off in Fig. 8. The SCE of SBTFET is suppressed due to the decrease in the depletion layer width from the source contact as illustrated in Fig.9. $I_{\rm D}$ - $V_{\rm G}$ and SS of short channel ($L_{\rm G}$ =10nm) SBTFET with various Na (Fig.10) show large Na is desirable for steeper SS as in the case of $L_{\rm G}$ =50nm. However contrary to the result for long $L_{\rm G}$, larger $\phi_{\rm B}$ is required for the realization of small SS (Fig.11). Figure 12 shows that the influence tendency of ϕ_B on SS and Ion/Ioff is totally changed between long and short $L_{\rm G}$ with the critical length of around 15nm. Considering large Ion/Ioff in short channel region (~10nm) and the uniformity against $L_{\rm G}$ fluctuation, we conclude that optimum ϕ_B exists around the mid-value of 0.61eV.

Conclusions

Device simulation of SBTFET revealed that low Schottky barrier and high channel carrier concentration is desirable for steep subthreshold swing due to the larger tunneling probability at source corner of the devices. For the short channel device however larger ϕ_B leads to the suppression of the SCE. As a total, optimum ϕ_B value exists in terms of the large *Ion/Ioff* ratio in short channel device and the characteristics uniformity against L_G fluctuation.

Acknowledgements

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Fig. 4 I_D - V_G and SS characteristics of SBTFET for various m* (Na=2x10¹⁹cm⁻³, ϕ_B =0.61eV)



various LG. Comparison between

Fig. 5 Band diagram and tunneling rate distribution at subthreshold region. (a) $\phi_B=0.81eV$,(b) $\phi_B=0.41eV$



Fig. 6 Band diagram and potential distribution for (a) Na = $5x10^{18}$ (cm⁻³), (b) Na = $2x10^{19}$ (cm⁻³)





Fig. 9 Band diagram of compare L_G for conventional FET and SBTFET



Fig. 12 SS and Ion/Ioff ratio as a function of L_G for various $\phi_B.$





