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Analysis and Modeling of Geometry Dependent Thermal Resistances in MOSFETs

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Abstract

It is demonstrated that the self-heating effect easily causes elevated thermal accumulation within the active device for thin substrate MOSFETs. This leads to a non-linearity of the thermal resistance, which originally is a material specific constant. Additionally, a compact model for describing the observed effective nonlinear thermal resistance has been developed which captures the device geometry effects as well as the bias condition dependences.

1. Introduction

The self-heating effect (SHE) of an integrated circuit (IC) is becoming a serious problem even at reduced bias conditions due to the extremely high device density of advanced ICs [1]. Elevated temperature within a device propagates all over the chip and increases its temperature [2]. The SHE is modeled with a thermal network which consists of a thermal resistance and a thermal capacitance for each device (see Fig. 1a). For accurate circuit simulation including the SHE, accurate estimation of these elements is inevitable. We focus here on the thermal resistance, because it is varied drastically according to device geometries.

The mechanism of the temperature propagation is studied with use of the SOI-MOSFET structure, where the silicon-layer thickness T_{SOI} and the BOX-layer thickness T_{BOX} are varied (see Fig. 1b). These two device-parameter variations allow the investigation of the SHE not only for the SOI-MOSFET, but also for bulk-MOSFET and DG-MOSFET as special limiting case.

2. Method and Results

2D-device simulations are performed for the investigation by assuming wide-width devices. The 2D-device simulators solve the thermal equation together with the electrical equations to consider the electro-thermal coupling in a consistent way [3]. However, how to set the thermal boundary conditions for the simulation determines the magnitude of the SHE as well as the temperature distribution within the device. We set the thermal contact at all the electrodes, where the heat transfer to the ambient air is neglected, to achieve similar self-heating effects as the measurements reported in [4]. Two different technology generations are studied as summarized in Table I.

The 1D thermal propagation from the hot spot by SHE to the substrate is written as [5]

$$\frac{d^2\Delta T}{dx^2} - \frac{hP}{\kappa A}\Delta T = 0 \qquad (1)$$

where ΔT is the excess temperature, h is the heat transfer coefficient, κ is the thermal conductivity, P and A are the perimeter and cross-sectional area of the diffusion region. The temperature distribution within the device is ignored. An analytical solution of eq. (1) is derived under the approximation that the lateral thermal diffusion is not hindered

$$R_{th0} = \frac{1}{2W}\cdot\frac{T_{BOX}}{\kappa_{OX}\left(L_h + L_g\right)}, \qquad L_h = \left(\frac{\kappa_{diff}T_{SOI}T_{BOX}}{\kappa_{OX}}\right)^{1/2} \qquad (2)$$

Here W and L_g are the channel width and length, and κ_{ox} and κ_{diff} are the permittivity of the oxide and the diffusion region. Eq. (2) is valid for a diffusion length L_{SD} longer than the thermal healing length L_h. Fig. 2a shows 2D-device simulation results of the thermal resistance R_{th} (=ΔT /power) as a function of T_{BOX}, depicted together with calculation results from eq. (2). The device dimensions are those of the device A in Table I, which are the same values in the device measurements reported in [4]. The case T_{BOX}=0 corresponds to the bulk-MOSFET. By increasing T_{BOX}, R_{th} increases, denoting the temperature increase within the device due to the thicker BOX which prevents thermal propagation to the substrate. The theoretical results roughly reproduce 2D-device simulation results without any fitting parameters. Fig. 2b shows results for the device B in Table I with thin T_{SOI}. The calculation results with eq. (2) don't fit to 2D-device simulation results any more but deviate substantially.

3. Discussions

With reduced T_{SOI}, the lateral thermal diffusion is suppressed as can be seen in the healing length L_h reduction (Table I). This intensifies heat accumulation within the active device. Eq. (2) is derived based on a simple 1D thermal propagation without inclusion of the heat accumulation [5]

$$R_{th} = \frac{T_{BOX}}{\kappa_{OX}\cdot 2A_{eff}} \qquad (3)$$

where A_{eff} is the effective conducting area. To extend eq. (2) for the heat accumulation condition we consider that the thermal healing length L_h increases when the thermal accumulation enhances as

$$R_{th,ac} = \frac{1}{2W}\cdot\frac{T_{BOX}}{\kappa_{OX}\left(L_h^{'} + L_g\right)}, \qquad L_h^{'} = L_h\cdot\left(\frac{T+\Delta T}{T}\right)^{1/2} \qquad (4)$$

It is approximated that the temperature increase within the active device is due to the thermal-resistance increase for the lateral heat diffusion, which is approximately written as

$$\frac{T+\Delta T}{T} = f\left(L_h/T_{SOI}\right) = \frac{1}{PWC}\cdot\frac{L_h}{T_{SOI}} \geq 1 \qquad (5)$$

where PWC is a model parameter corresponding to the power translating to a thermal resistance. Calculation results with PWC=10 are depicted (dashed lines) in Fig. 2b together with the original results (solid lines). The results are satisfactory.

Fig. 3a shows 2D-device simulation results of temperature increase ΔT vs. power applied for the device A with T_{SOI}=177nm, and Fig. 3b for the device B with T_{SOI} =20nm. For the device A, linear dependences are observed for all studied cases, whereas non-linear dependences are detected for the device B. It is expected that the nonlinear temperature increase is induced by the heat accumulation within the device. Fig. 4 compares the thermal resistance R_{th} of 2D-device simulation results for the devices A and B as a function of the drain voltage V_{ds}. For the device B, where the heat accumulation occurs, the expected non-linearity of R_{th} is obtained. Compact modeling of the characteristics is done with use of R_{th} including heat accumulation $R_{th,ac}$ as

$$R_{th} = R_{th,ac} + \left(R_{th0} - R_{th,ac}\right)\left(I_{ds}V_{ds} - PW0\right), \quad I_{ds}V_{ds} - PW0 \geq 0 \quad (6)$$

The model parameter $PW0$ denotes the threshold for heat accumulation. Model results with $PW0$=0.1 are summarized in Fig. 5 together with 2D-device simulation results.

3. Conclusion

The thermal propagation within a MOSFET device was investigated with 2D-device simulations. An analytical compact-model description of the thermal resistance was derived as a function of device geometry as well as the bias conditions. Good compact-model agreement is verified for different device geometries as well as bias conditions.

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References

[1] B. Tenbroek, *et al.*, IEEE J. Solid-State Circuits **33** (1998) 1037.

[2] K. Ishiguro, *et al.*, in ICMTS Tech. Dig. (2012) 187.

[3] ATLAS by Silvaco & SENTAURUS by Synopsys.

[4] L. T. Su, *et al.*, IEEE Trans. on Elec. Dev. **41** (1994) 69.

[5] B. Behkam, *et al.*, Int. J. Heat and Mass Transfer **48** (2005) 2023.

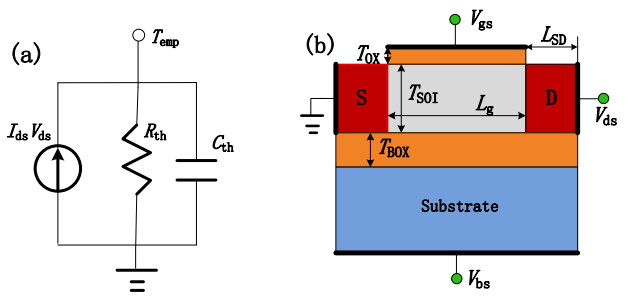

Fig. 1. Schematic of studied (a) thermal network and (b) SOI-MOSFET structures.

Table I. Device parameters studied.

Device	A	B
T_{OX}	5.5nm	2nm
T_{SOI}	177nm	20nm
V_{gs}=V_{ds}	1.5V	1.1V
L_{SD}	1.5um	1.5um
L_h	1.99um	0.67um

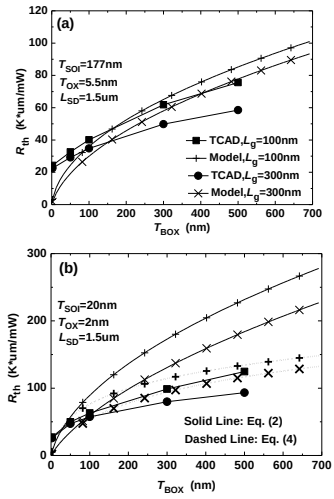

Fig. 2. Comparison of model calculation results of the thermal resistance R_{th} with those of 2D-device simulation results (a) for the device A and (b) for the device B shown in Table I.

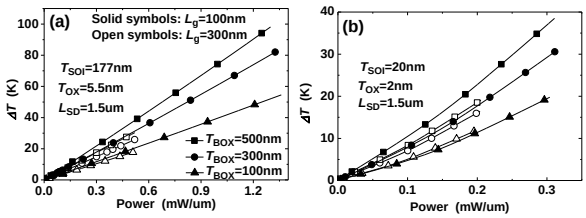

Fig. 3. 2D-device simulation results of temperature increase ΔT as a function of power (a) for the device A and (b) for the device B.

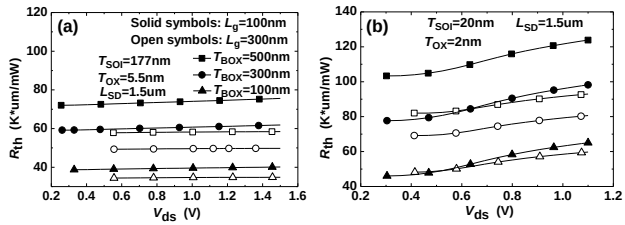

Fig. 4. 2D-device simulation results of the thermal resistance R_{th} as a function of V_{ds} (a) for the device A and (b) for the device B.

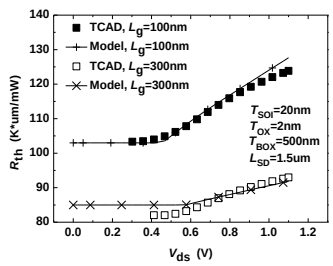

Fig. 5. Comparison of calculated R_{th} with eq. (6) to 2D-device simulation results for the device B.