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The investigation on Dislocation Edge Stress Effects for Si N-MOSFETs

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1. Introduction

Single-directional Solid Phase Epitaxial Re-growth (SPER) process of amorphous Si has been a topic of fundamental and technological importance for several decades since first being reported more than 40 years ago [1, 2]. The roles of growth temperature [3], substrate orientation [4], and impurities [5] had also been widely studied with more investigation of these effects of stress on the single-directional SPER process [6]. In addition to the single-directional process, Dr. Morarka and Dr. Rudawski has also studied and reviewed the two-dimensional (2D) SPER process recently [7, 8], because SPER process must be considered as multi-directional rather than bulk in nature with the evolving growth interface having multiple crystallographic orientations in the modern patterned device processing. For the 2D SPER process, the relative differences in the velocity of re-growth fronts with different multiple crystallographic orientations and intrinsic stress induced from the typical Si-based device fabrication will lead to the formation of device mask edge defects [7]. The experimental data show that the stress generated in the Si substrate from the patterning, both in line and square structures, alters the kinetics and geometry of the multi-directional SPER process, and can influence the formation of mask edge defects which form during the growth to different degrees as per difference in the substrate stresses generated by each type of patterning [8]. On the other hand, some other research groups [9] in the company recently found that these mask edge dislocation defects, introduced from amorphization implants and subsequent SPER process, have been shown to induce tensile-like stress in the channel of the Si transistor resulting in NMOSFETs mobility enhancement, based on the strained Si theory [10-12]. However, the detailed mechanism for the root cause of tensile-like stress in the channel by SPER process and a numeric model for the mask dislocation edge stress are still unclear and lacked. In this work, the AFM-Raman technique with the nanometer (nm) level space resolution to extract the channel stress in the real transistor dimension is carried out firstly. Secondly, the measured stress is compared with the simulation model by the proposed finite element method in this work to evaluate realistic devices with surfaces and material interfaces. After the calibration and the agreement between simulation data and experimental electrical characteristics of the real transistor, the physical origin and simulated model for the dislocation edge stress on the real application for the transistor performance booster have been understood and given, respectively. Finally, the optimal dislocation shape, including dislocation length and angle, is also discussed and proposed in this work, based on the understanding of dislocation edge stress.

2. General Instructions

Fig. 1 shows the traditional transistor structure with and without the dislocation edge stress treatment. As the study in our previous work [13], the high compressive stress in Si OD region can be observed during the processed thermal budget in the modern semiconductor manufacture, due to the difference of the thermal expansion coefficient between Si and STI oxide. As the device dimension continuously scaling down, the compressive stress in Si OD becomes larger and further degrades the electron carrier mobility and the N-MOSFET device performance. With the heavy ion implant in the S/D region and following SPER process, the mask edge dislocation line will be formed near the source and drain region as shown in Fig. 1, due to the different re-growth/crystal velocities between <001> and <110> directions in the amorphous Si region. The detailed mechanism for the dislocation line formation with different process conditions including ion implant dosage, ion implant energy, thermal budget conditions, the shape of the spacer, and mask layout can be referred to Ref. 7 and 8.

Fig. 2 shows the AFM-Raman spectra in the real transistor OD size about 50 nm X 50 nm on three samples: Sample A: Blanket/unstrained Si wafer to do the reference and standard for the Si-Si phonon at 521 cm^{-1}. Sample B: The Si transistor with traditional process, and Sample C: The Si transistor with dislocation edge stress treatment. When we compare the AFM-Raman spectra between Sample A and Sample B, it shows that there have about 3.5 cm^{-1} wave-number shift from 521 cm^{-1} to 517.5 cm^{-1}. It indicates that the Sample B has the corresponding compressive stress ~1 GPa in Si OD after the calculation on the dependency between Raman wave-number shift and stress [13, 15, 16]. In addition to the usage of one-side pad SiN layer to relax the STI compressive stress, proposed by our previous work [13], Sample C is also been found that it has the less Raman wave-number shift (~2 cm^{-1}) and less compressive stress (~0.4 GPa) in Si OD. It shows that the dislocation edge line near the source and drain region can relax the STI compressive stress in the channel.

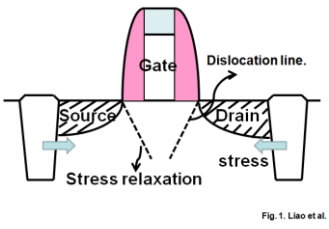

Fig. 1. Liao et al.

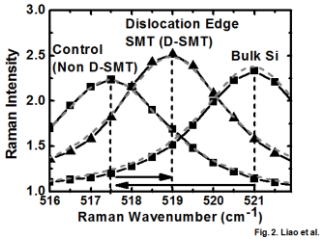

Fig. 2. Liao et al.

Fig. 1 The traditional transistor structure with and without the dislocation edge stress treatment.

Fig. 2 AFM-Raman spectra on three samples: Sample A, Sample B, and Sample C.

Fig. 3 shows the comparison of the stress between experimental AFM-Raman extraction and the modeling by finite element method on both samples: Sample B (The Si transistor with traditional process) having ~1 GPa compressive stress and Sample C (The Si transistor with dislocation edge stress treatment) having ~0.4 GPa compressive stress along the gate length direction. The dislocation edge process indeed can relax the STI compressive stress and the simulated model agrees well with the experimental data extracted by AFM-Raman. The calibrated simulation model can help us a lot for the further stress design and optimization with different dislocation edge stress process treatments.

Fig. 4 compares the electrical data with the dislocation edge stress process treatment from Ref. 9 and the theoretical calculation on the electron mobility dependency with the channel stress from our work in Ref. 10-12. With the calibration among measured stress data by AFM-Raman, simulated stress value by finite element method, and its corresponding electrical characteristics, the full simulated model on the characteristics of transistor with the dislocation edge stress treatment are created and provided successfully.

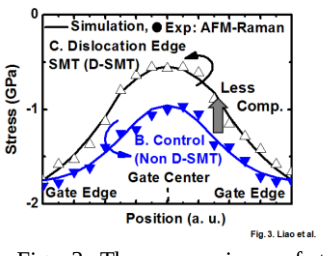

Fig. 3. Liao et al.

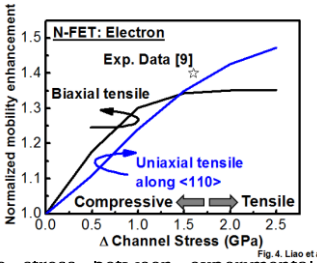

Fig. 4. Liao et al.

Fig. 3 The comparison of the stress between experimental AFM-Raman extraction and the modeling.

Fig. 4 The comparison between the electrical data with the dislocation edge stress process treatment from Ref. 9 and the theoretical calculation.

Based on the simulation model developed in this work, the different dislocation edge shapes are further investigated in Fig. 5, including the effect for the length of dislocation line in Fig. 5(a) and the effect for the angle of dislocation line in Fig. 5(b). It can be found and needed to point out that the longer length of the dislocation line and smaller angle of the dislocation line has the better performance to relax the compressive stress in Si OD from STI and let the Si OD stress toward more tensile-like (Case B in Fig. 5 (a) and Case A in Fig. 5 (b)). The different shape of dislocation edge line can be achieved by designed semiconductor process conditions such as ion implant dose, ion implant energy, the edge shape of the spacer, the layout of the mask, and process thermal condition.etc., which has been investigated in Ref. 7 and 8..

3. Conclusions

In a summary, the comprehensive study on the dislocation edge stress to relax the compressive stress from STI and enhance the electron carrier mobility are presented in this work with the accurate stress measurement by AFM-Raman and proposed simulation model. The AFM Raman technique provides the method to extract the Si OD stress with the nm level space resolution. Less compressive stress in Si OD from STI with the dislocation edge stress treatment measured by AFM Raman spectra agree well with the simulation model and has the reasonable corresponding mobility enhancement. Based on the calibration of the simulated model on the dislocation edge stress, we can further found that the longer length of dislocation line and smaller angle of dislocation line can further relax more compressive stress in Si OD from STI and should contribute more electron mobility improvement in NMOSFETs.

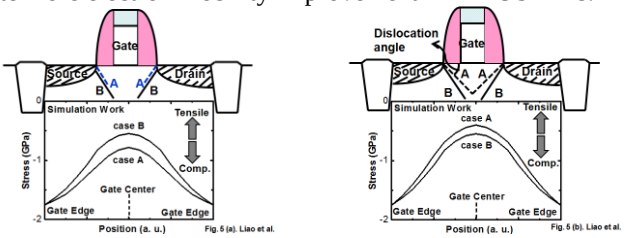

Fig. 5 The simulated stress dependency with dislocation edge shape, including the length of dislocation line in Fig. 5 (a) and the angle of dislocation line in Fig. 5 (b).

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