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A Simple Circuit to Investigate Threshold Voltage Variation and Its Application in Monitoring NBTI Degradation

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1.Introduction

With IC industry improving and device scaling, reliability is becoming more serious. The Negative Bias Temperature Instability (NBTI) is a main degradation mechanism in p-MOSFET devices. Under negative voltage bias and elevated temperature, more interface traps generate and cause the threshold voltage shift [2]. When the threshold voltage shifts, drain current and transconductance for p-MOSFETs reduce, which are considered as major reliability issues in digital and analog IC. Such degradation shortens the device lifetime, and even influences the whole integrated circuits. At the same time, device scaling means more MOSFET devices on a chip. The critical parameters play an important role in the time-based reliability [3]. Therefore it is necessary to test and analyze the threshold voltage mismatch before MOSFET devices are put into use. Some V_T extractor realizations have been published [4-7]. An array-based structure for measuring the electrical property of large numbers of MOSFETs is also proposed in [8]. In this paper, we report a simple circuit for the measurement of threshold voltage shift and fluctuation, which can monitor the NBTI degradation directly and effectively. The characteristics of the circuit and the simulation results are then discussed.

2.General Instructions

Circuit implementation and analysis

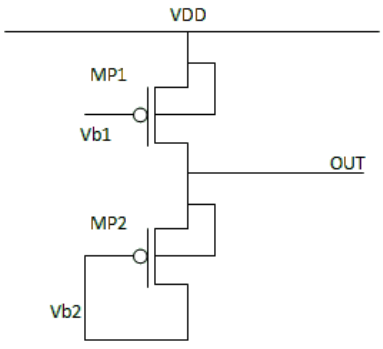

Fig.1 Proposed circuit structure.

Fig.1 shows the proposed circuit structure, including two p-MOSFETs, in series. In our experiment, MP1 and MP2 have the same channel length and aspect ratios (i.e. W/L=4/1). In the 65nm technology, the voltage supply V_{DD} is designed as 1.2V. We have saturation region current expressions of MP1 and MP2

$$I_{p1,2} = \frac{1}{2}\mu_p \frac{W}{L} c_{ox}(V_{GS1,2} - V_{TH1,2})^2 \qquad (1)$$

If MP1 experiences NBTI degradation, the change of $(V_{GS1} - V_{TH1})$ is determined by threshold voltage (V_{TH1}) when MP2's is determined by output voltage (V_{OUT}). Considering MP1 have the same drain current with MP2, it is clear the difference between threshold voltages of MP1 and MP2 is presented in the output node, if V_{b1} and V_{b2} are constant. Considering the threshold voltage of PMOS transistor for the used technology is less than 400mV, we design V_{b1}=700mV and V_{b2}=200mV. Thus, we finally get

$$V_{TH1} - V_{TH2} = V_{OUT} - 700\text{mV} \qquad (2)$$

And we get the relationship between the absolute value of shift of MP1 threshold voltage (ΔV_{TH1}) and output voltage shift (ΔV_{OUT}) (i.e. $\Delta V_{TH1} = \Delta V_{OUT}$). Using the proposed circuit, we can monitor the shift of PMOS threshold voltage by direct output voltage measurement.

Simulation results and discussions

To verify this method, an HSPICE simulation was conducted for different PMOS transistors, whose channel lengths range from 80nm to 400nm. The relationship of output voltage shift (V_{OUT}) and ΔV_{TH1} are shown in Fig.2.

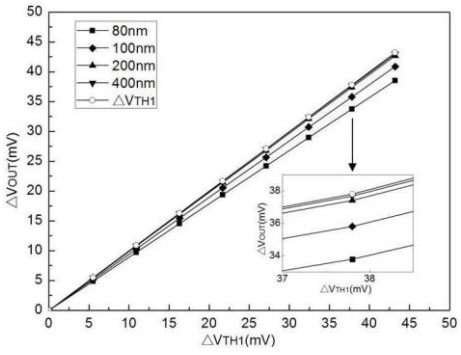

Fig.2 The relationship between ΔV_{OUT} and ΔV_{TH1}.

Here, we assume ΔV_{TH1} shifts from 0mV to 45mV, it is observed that ΔV_{OUT} is proportional to the threshold voltage shift, and ΔV_{OUT} are always less than ΔV_{TH1}. The deviation is getting smaller and smaller with the increasing of channel length. To short channel devices, channel length modulation plays an important role in the deviation. Other second-order effects such as mobility degradation have the same impact on ΔV_{OUT}. When the channel length increases, second-order effects become less serious. The decline of V_{OUT} follows the shift of V_{TH1} more accurately.

The NBTI model can be found on the PTM website [1]. In stress phase, ΔV_{TH} may be expressed as:

$$\Delta V_{th} = \sqrt{K_v^2 (t - t_0)^{0.5} + \Delta V_{th1}^2} + \delta_v \qquad (3)$$

where $K_v = AT_{ox}\sqrt{C_{ox}(V_{gs}-V_{th})}\exp\left(\frac{E_{ox}}{E_0}\right)\cdot [1-\frac{V_{ds}}{\alpha(V_{gs}-V_{th})}]\exp(\frac{-E_{ox}}{E_0})$ (4)

and $E_{ox} = (V_{gs}-V_{th})/T_{ox}$ (5)

The parameter values were chosen from the 65nm NBTI model proposed in [1]. From eq. (3), ΔV_{th} is proportional to $t^{1/4}$, where t means time. We simulate the NBTI degradation with time in 200nm channel length p-MOSFET, shown in Fig. 3.

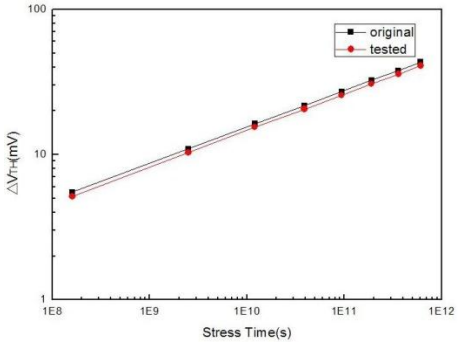

Fig.3 The threshold voltage NBTI degradation with time.

Therefore, with second-order factors taken into account, the circuit reflects the shift of V_{TH1} in the output voltage. Within the simulation range, the channel length induce measurement error is less than 10%.

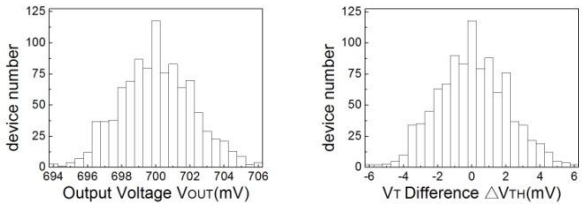

Fig.4
a The V_{OUT} distribution b The V_T distribution

Since the circuit is designed to monitor the shift of V_{TH1} in output node, it can be applied to the measurement of threshold voltage fluctuation of the p-MOSFET devices also. From eq. (2), the difference between the threshold voltages of MP1 and MP2 (ΔV_{TH}) can also be measured in output node. If we take MP2 as an ideal device, the mismatch of p-MOSFET devices in the position of MP1 is easily observed. The distribution of output voltages for 1000 p-MOSFET devices is shown in Fig.4a. Compared with the 1000 p-MOSFET devices threshold voltage distribution, shown in Fig.4b, it is easy to find that the proposed method can predict the threshold voltage distribution of large numbers of p-MOSFET devices accordingly.

The simulation results above are based on the ideal case of MP2. However, MP2 is also a PMOS chosen from a mass of p-MOSFET devices. The threshold voltage of MP2 itself may have some shift from standard design. The dependence of output voltage distribution and threshold voltage shift of MP2 (ΔV_{TH2}) is obtained, shown in Fig.5.

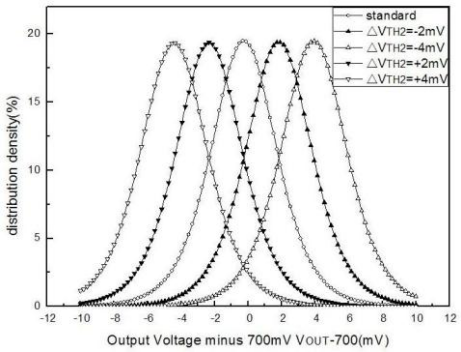

Fig.5 The dependence of output voltage distribution and threshold voltage shift of MP2 (ΔV_{TH2})

It is obvious that the output voltage remains normal distribution with the same standard deviations and different expectations, when V_{TH2} is changing from standard design. Therefore, the proposed method could realize the function of statistically testing threshold voltage fluctuation.

3.Conclusion

A circuit testing p-MOSFET V_{TH} shift and fluctuation is proposed. Under a proper voltage bias, the circuit could reflect the NBTI degradation of PMOS V_{TH} in output node. The method has been presented more than 90% accuracy with various channel length devices in 65nm technology. Moreover, the method could also be used to obtain the threshold voltage fluctuation of p-MOSFET devices. This simple structure offers a solution to directly measure the threshold voltage shift and mismatch of p-MOSFETs.

Acknowledgements

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References

[1] PTM web site http://www.eas.asu.edu/ptm/

[2] S.V. Kumar, K.H. Kim and S.S. Sapatnekar, "Impact of NBTI on SRAM Read Stability and Design for Reliability," ISQED, 2006, pp. 213-218

[3] W. Wang, V. Reddy, A. T. Krishnan, R. Vattikonda, S. Krishnan, and Y. Cao, "Compact modeling and simulation of circuit reliability for 65-nm CMOS technology," IEEE Trans. Device Mater. Rel., 2007, **7**, (4), pp. 509–517

[4] S. Vlassis and C. Psychalinos, "Low-voltage CMOS V_T extractor," Electron. Lett., 2007, **43**, (17), pp. 921-923

[5] N. Manaresi, E. Franchi, A. Gnudi and G. Baccarani, "MOSFET threshold extraction circuit," Electron. Lett., 1995, **31**, (17), pp. 1434-1435

[6] C.G. Yu and R.L. Geiger, "An accurate and matching-free threshold voltage extraction scheme for MOS transistors," Proc. IEEE Int. Symp. On Circuits and Systems, May 1994, Vol. **4**, pp. 115-118

[7] G. Fikos and S. Siskos, "Low-voltage, low-power, accurate CMOS V_T Extractor," IEEE Trans. Circuits Syst. II, 2001, **48**, (6), pp. 626-628

[8] S. Watabe, S. Sugawa, K. Abe, T. Fujisawa, N. Miyamoto, A. Teramoto and T. Ohmi, "A test structure for statistical Evaluation of characteristics variability in a very large number of MOSFETs," in Proc. IEEE Int. Conf. Microelectron. Test Struct., 2009, pp. 114–118.