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Superior Recovery Characteristics of SiGe pMOSFETs under NBTI Stress

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1. Introduction

SiGe channel is one of the most promising candidates as a performance booster for pMOSFETs because of its high hole mobility and compatibility with conventional CMOS processes [1]. Negative-bias temperature instability (NBTI) is considered to be a major reliability issue for scaled CMOS technologies due to the increased oxide electric field (E_{ox}) caused by scaled electrical oxide thickness (EOT). Many investigations on the NBTI of SiGe pMOSFETs have only focused on degradation characteristics [2], [3], and there are a few papers describing the recovery characteristics of the devices. Under real operating conditions, however, the devices would be subjected to repeated stress and recovery phases. In this study, we investigate the degradation and recovery characteristics of SiGe pMOSFETs with an HfO_2/TiN gate stack under NBTI stress and compare them with those of control Si pMOSFETs. We report the improved recovery characteristics of SiGe pMOSFETs and their superior NBTI reliability under real operating conditions.

2. Experiments

SiGe/Si heterojunction pMOSFETs were fabricated using a standard 45 nm gate-first CMOS flow on 8-inch n-type Si (100). A SiGe epitaxial layer was grown by ultrahigh vacuum chemical vapor deposition (UHVCVD) on an n-type Si. The thickness of the SiGe epitaxial layer and the concentration of Ge were optimized to 5 nm and 25%, respectively. A 3 nm Si-cap layer was deposited to encapsulate the SiGe layer. TiN and HfO_2 were used for the gate metal and dielectric, respectively. Conventional Si pMOSFETs having the same gate structure were also fabricated for comparison.

3. Results and Discussion

The degradation and recovery characteristics of SiGe and Si pMOSFETs were investigated under various NBTI stresses. Fig. 1 shows the threshold voltage instability (ΔV_{th}) versus stress time characteristics for both pMOSFETs at 125 °C. Both pMOSFETs were subjected to E_{ox} of 9 MV/cm during the stress phase, and to V_g of 0 V during the recovery phase. The SiGe pMOSFET showed lower ΔV_{th} than the Si pMOSFET, which was due to the lower tunneling probability induced by a quantum well channel structure with a quantum mechanical barrier of the Si cap at the SiGe/Si heterojunction [3]. It is noted that the SiGe pMOSFET also showed a higher percentage of recovery (R) (defined as (ΔV_{th} (500 s) - ΔV_{th} (1000 s)) / ΔV_{th} (500 s)) than that of the Si pMOSFET. To investigate the superior recovery characteristic of the SiGe pMOSFET, its dependence on the stress conditions was investigated in Fig. 2. The ΔV_{th} of both devices was measured under various stress E_{ox} and temperatures (T) but under the same recovery condition of V_g = 0 V. In Fig. 2(b), however, T at the recovery phase necessarily varies as the stress T varies. For both devices, R decreased linearly as E_{ox} increased, yet R has relatively little dependence on T. These results indicate that the recovery of both devices is dominated by identical field-activated process. If using high-k dielectrics, recoverable ΔV_{th} mainly occurs by the charge trapping to preexisting traps of the high-k layer, and a great deal of the recovery occurs within a second [4]. In Fig. 3, the strong dependence of R on E_{ox} is separately analyzed using the fast recovery (FR) and slow recovery (SR) component, in which FR is defined as the recovery during the first second of recovery time and SR is defined as the remainder of the total recovery. For both devices, the FR component had almost the same E_{ox} dependence as the total recovery, and the SR component showed a weak E_{ox}-dependent characteristic; this indicates that the strong E_{ox} dependence of R is due to the FR process. In addition, the strong E_{ox} dependence of FR and the weak temperature dependence of R in Fig. 2(b) indicate that the FR occurs through the tunneling process of trapped charges, from bulk traps to the channel [5]. As the E_{ox} decreases, R rapidly increases and most of the recovery occurs through the FR process. Therefore, in low E_{ox} conditions which are close to real operating conditions, the FR process governs the recovery behavior of both pMOSFETs, and the improved R of SiGe pMOSFETs would be due to an improved FR process. The dependence of FR on E_{ox} in SiGe pMOSFET could be explained by an energy band diagram shown in Fig. 4 if assuming the existence of a defect band of hole trap precursors. The defect band of preexisting traps of HfO_2 accessbile to channel carriers varies depending on E_{ox}. Under relatively high E_{ox}, the defect band becomes wider than under a low E_{ox} condition, and more channel carries are captured in the dielectric. It is noted that the defect band for high E_{ox} contains the defect band for low E_{ox}, and that the increased portion is located further away from the

Fermi level at the recovery condition than is the defect band for low E_{ox}. As a result, the FR probability of trapped charges in the increased portion of the defect band at high E_{ox} is lower than that of trapped charges under low E_{ox}, because the FR occurs through a tunneling process [5]. As shown in Fig. 5, therefore, as stress E_{ox} increases or ΔV_{th} increases, the percentage of FR of trapped charges decreases; this situation is the same for the Si pMOSFET. It is noted that the SiGe pMOSFET showed the lower percentage of FR at similar ΔV_{th}, which was probably due to the low tunneling probability to the buried quantum well channel structure. Therefore, the higher FR and R of the SiGe pMOSFET after the same E_{ox} stress are mainly attributed to the device's lower degradation characteristic.

3. Conclusions

The degradation and recovery characteristics of SiGe pMOSFETs with an HfO_2/TiN gate structure were investigated under NBTI stress. The SiGe pMOSFETs showed improved recovery characteristics than the Si pMOSFETs, which was mainly attributed to their lower degradation characteristic. As E_{ox} decreases, a great deal of ΔV_{th} would rapidly recover through the FR process and newly-generated interface traps would lead to permanent damage and determine the degradation level of V_{th}. Therefore, the fabrication of high quality interface with resistance to stress is essential to ensure reliable NBTI characteristics of SiGe pMOSFETs.

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References

[1] J. Mitard et al., IEDM Tech. Dig. (2010) 249.
[2] J.-S. Yuan et al., Microelectron. Reliab. **51** (2011) 914.
[3] J. Franco et al., Pro. of IRPS (2010) 1082.
[4] B. H. Lee et al., Jpn. J. Appl. Phys. **44** (2005) 2415.
[5] D. Heh et al., IEEE Elec. Dev. Lett. **29** (2008) 180.
[6] S. Zafar et al., IEEE Trans. Dev. Matter. Reliab. **5** (2005) 45.
[7] G. Groeseneken et al., IEEE Trans. Dev. Matter. Reliab. **31** (1984) 42.
[8] M. S. Park et al., IEEE Elec. Dev. Lett. **31** (2010) 1104.
[9] J. Franco et al., IEDM Tech. Dig. (2010) 70.

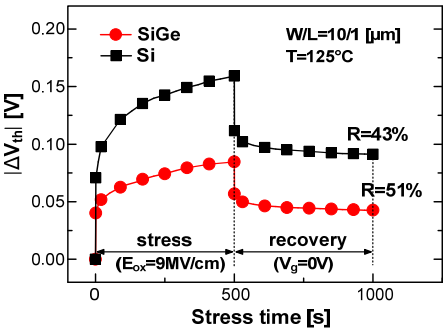

Fig. 1. ΔV_{th}-t characteristics of SiGe and Si pMOSFETs at 125 ºC.

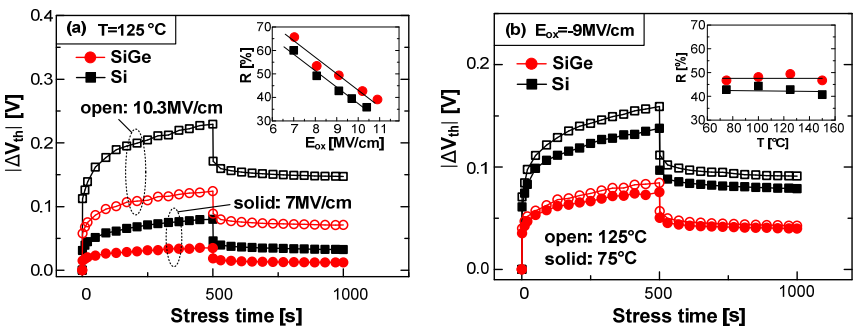

Fig. 2. Dependence of the degradation and recovery characteristics on (a) E_{ox} and (b) temperature. Insets show dependence of R on (a) E_{ox} and (b) temperature.

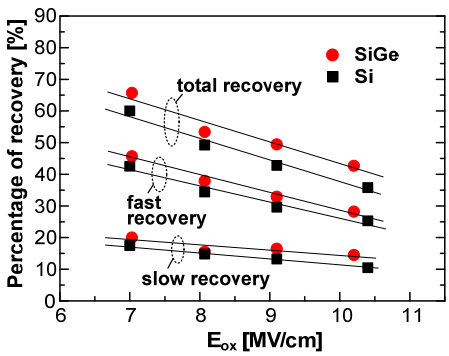

Fig. 3. Field dependence of fast, slow and total recovery.

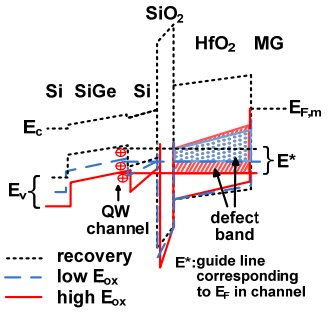

Fig. 4. Energy band diagram corresponding to recovery, low, and high E_{ox} conditions (only E_v is described for low and high E_{ox} conditions).

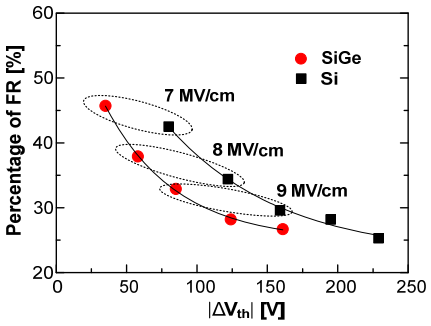

Fig. 5. Dependence of percentage of FR on ΔV_{th}.