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Effect of Anneal Process on Trap Properties in Metal/High-k Gate MOSFETs through RTN Characterization

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1. Introduction

In order to understand the trap properties in small-area devices, random telegraph noise (RTN) becomes much more important, owing to the capture and emission of a single carrier at a gate dielectric trap [1]. Although some works have been studied on the trap behavior of high-k dielectrics, relatively little literature has focused on the anneal-dependent trap position that could be linked to the oxygen-passivated mechanism. In this letter, the RTN phenomenon of high-k nMOSFETs with different post-metal anneal conditions is investigated in comparison with devices without annealed.

2. Experiment

A 20 Å Hf-based dielectric film was deposited on an ultra-thin SiO_2 film (~1.0 nm) by atomic layer deposition (ALD). Then, a thin TiN layer was as a barrier layer for oxygen out-diffusion [2]. After the poly-Si gate was removed, three types of device were fabricated with same structures except anneal sequences. Devices with TiN annealed mean that the samples followed by a PMA treatment. After poly-Si removing, it was followed by a thin TaN layer. Here the samples with the same PMA treatment were called TiN/TaN annealed. For comparison, the samples fabricated without any PMA treatment were called as deposited. And the DC and RTN characteristics of the samples were analyzed with Agilent B1500A semiconductor parameter analyzers.

3. Results and Discussion

The I_{DS}-V_{DS} characteristics of nMOSFET devices with three types of annealing conditions are shown in Fig. 1. As shown, nMOSFETs with a dual-metal-layer anneal shows an approximately 4% I_{DS} improvement as compared to the devices.

The extracted mean capture (τ_c) and emission (τ_e) time constants, respectively in the high- and low-current states as shown in Fig 2, within a gate overdrive rang of -0.1 V to 0.4 V are presented in Fig. 3. RTN phenomenon appears at high voltage in the samples with a dual-metal-layer anneal, and it implies that electrons are minor captured. By analyzing the gate bias and drain dependences of the time constants as shown in Fig. 4, one can determine trap depth (x_T), i.e. the distance from the Si/SiO_2 interface, determined by the slope of line with equation (1) [3]:

$$\frac{\partial \ln(\tau_c / \tau_e)}{\partial V_{GS}} = \frac{-q}{kT}\left(\frac{x_T}{t_{ox}}\right) \qquad (1)$$

where t_{ox} is the physical thickness of the gate oxide, and k is the Boltzmann constant. Interestingly, the location of the defects in samples with a dual-metal-layer anneal approaches the interface of high-k dielectric and interfacial layer (IL) and so does as deposited, while the x_T for devices with mono-metal-layer anneal is 2.7 nm, which is within the high-k layer. The closer proximity to the IL/Si interface will be responsible for the reduced tunneling attenuation length (λ) for 1/f noise characterization.

By using band gap, electron affinity, thickness, and dielectric constant of metal/HfO_2/SiO_2/Si structure, energy band diagram can be built [4] as shown in Fig. 5(a). Dash lines present energy levels at high gate voltage, and the dependence of gate voltage and trap energy for different trap depths is shown in Fig. 5(b)-(d), respectively. As trap energy (E_T) equals to Fermi level (E_F) of Si, electron trapping is increasing. On the other hand, RTN phenomenon disappears due to discordance of E_T and E_F. Band diagrams in different samples are determined by the difference of basic line (initial E_T) and the volume of voltage variation (ΔE_T). While varied gate voltages during the same range in samples with a mono-metal-layer anneal will cause the most part of variation in E_T below E_F, as depicted in Fig. 5(b), and it limits the RTN phenomenon at high voltage overdrive observed in Fig. 4. On the contrary, samples with a dual-metal-layer anneal encompass smaller difference between vacuum level (E_{VAC}) and trap energy ($\Delta E_{VACT} = E_{VAC} - E_T$) and shallower trap depth that causes the most part of variation in E_T above E_F, as depicted in Fig. 5(d), this confirms that RTN phenomenon appears at high gate voltage in Fig. 4.

The variation of trap depth depending on anneal conditions can be understood with Fig. 6. Due to the negative enthalpy of oxygen atoms reacting with nitrogen vacancies, it makes nitrogen defects filled and even they replace the nitrogen ions in TiN. Therefore, the replaced nitrogen ions form new defects in dielectric after annealing, as shown in Fig. 6(b), which is consistent with the simulation results [5]. Nitrogen ions existed in HfO_2 will increase electron trapping, as in SiO_2 [6], and induce the trap location closer to the interface between TiN and HfO_2, as confirmed by Fig. 4. Similarly diffusion mechanism for devices with dual-metal-layer anneal is shown in Fig. 6(c). Particularly, the nitrogen defects in TiN layer will be passivated, whereas causes the trap location is near HfO_2/IL interface. Furthermore, the passivation of TiN reduces

electron trapping and increases drain current for device with dual-metal-layer anneal as shown in Fig. 1.

4. Conclusions

In mono-metal-layer annealed samples, nitrogen ions replaced by oxygen ions induces new defects in dielectric and increases trap depth based on RTN analysis. However, current enhancement in dual-metal-layer annealed samples is due to that passivation of TiN layer and decreases the opportunity of electrons to be trapped.

Acknowledgements

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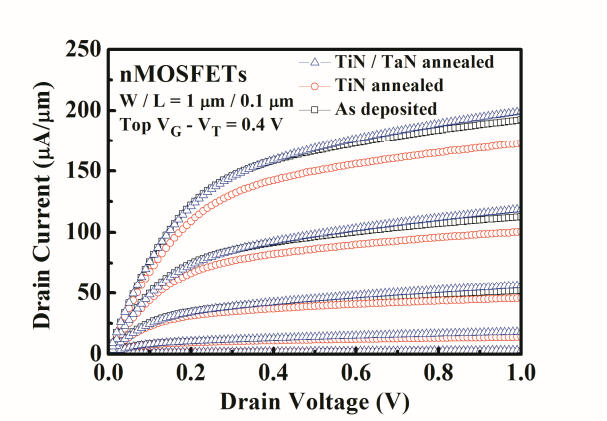

Fig. 1 Drain current versus voltage as function of gate overdrive voltage.

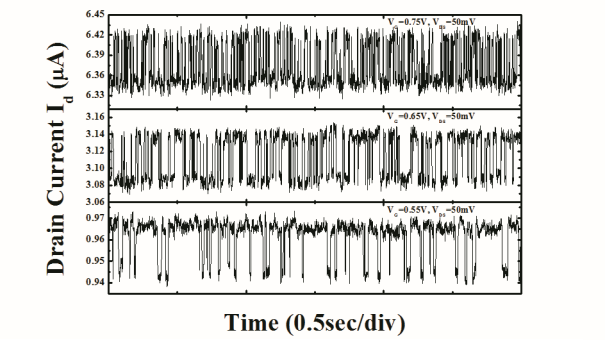

Fig. 2 Drain current as a function of time for varying gate bias.

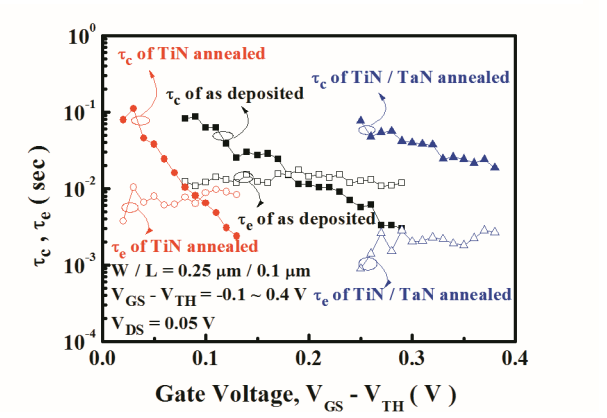

Fig. 3 The dependence of τ_c (solid point) and τ_e (hollow point) on (V_{GS}-V_{TH}) for different annealing conditions.

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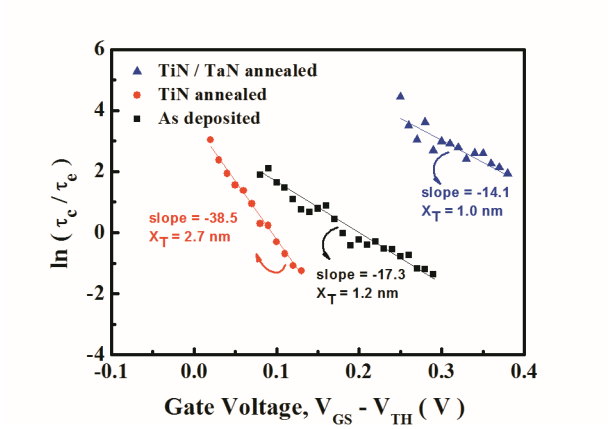

Fig. 4 The value of $\ln(\tau_c / \tau_e)$ varies with respect to gate voltage overdrive.

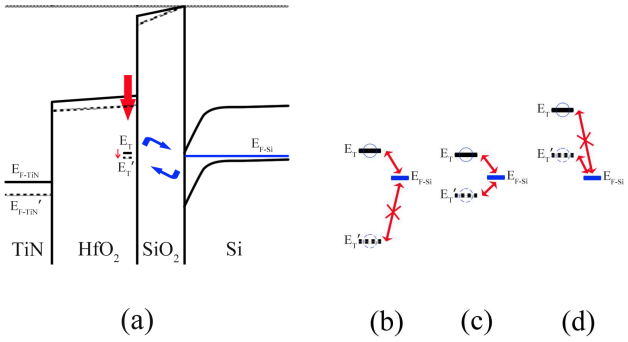

Fig. 5 Energy band diagram of traps by increased electric field. (a) Oxide traps in HfO_2 are observed in inversion modes and interact with channel. For different processes: (b) TiN annealed; (c) without oxygen annealing; (d) TaN/TiN annealed.

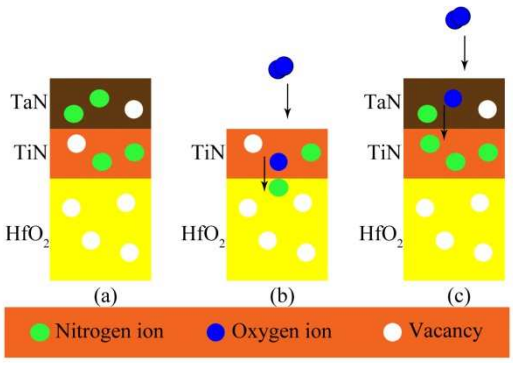

Fig. 6 Schematic illustration for the process of nitrogen ions replace by oxygen ions in TaN/TiN stack.