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# Characterization of Oxide Traps in 28 nm nMOSFETs with Different Uniaxial Tensile Stress by Utilizing Random Telegraph Noise (RTN)

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## 1. Introduction

Way of optimizing channel mobility need to be explored in order to overcome the limitations on the scaling down of devices and to further improve the speed of CMOS circuits. Channel strain engineering is currently one of the most promising candidates to reach this demand and to maintain the MOS performance improvement trajectory laid out in the ITRS roadmap. The benefits of uniaxial strained technology are the low cost flow and effective improvement of n- [1] and p-type [2] device performance even in a small area, which results from the strained-induced reduction of effective mass and scattering. Using stress-memorization technique (SMT) has also been reported to further improve the nMOSFET performance [3, 4]. As strain engineering have been commonly incorporated in the CMOS technologies to enhance the device performance, the 1/ *f* noise is being considered regarding continuously scaling down CMOS devices due to the 1/ *f* noise increases as the reciprocal of the device area. Moreover, 1/ *f* noise is also a viable characterization tool that used in the area of Si MOSFETs to examine interfacial physics. However, it is inadequate for small area devices (< 1 $\mu m^2$) because there is existed larger noise level variation between the samples-to-samples [4]. In order to understand the trap property in small-area device, random telegraph noise (RTN) becomes much more important due to the capture and emission of single carrier at a gate dielectric trap [5]. In this paper, we explore the RTN in drain current of 28-nm node nMOSFETs with different SMT film thickness, and investigate the physics-based properties of traps locations in the dielectric layer.

## 2. Device Structure and Experiment

The strained Si nMOSFETs used in this study were fabricated by 28-nm technology CMOS process sequence is illustrated in Fig. 1. The uniaxial tensile SiN of 100Å (Device A), 200 Å (Device B) and 300 Å (Device C) were deposited as SMT film by plasma-enhanced chemical vapor deposition (PECVD). The measured RTN was made by Waveform Generator / Fast Measurement Unit (WGFMU) measurement system based on Agilent B1500 Semiconductor Parameter Analyzer and measured in the drain current fluctuation of gate width (W) × gate length (L) = 0.25 ×0.04 $\mu m^2$. Six devices were measured in order to avoid singular effects and demonstrate the reproducibility of the oxide trap characterization.

## 3. Results and Discussion

Figure 2 shows the drain current ($I_{DS}$) as a function of drain voltage ($V_{DS}$) for nMOSFETs. Around 18% and 8% $I_{DS}$ enhancement for Device C and Device B were observed, compared to the Device A at a fixed gate overdrive, $V_G - V_T = 0.8$ V, and $V_D = 1.0$ V, which clearly indicates the SMT process can efficiently induce tensile strain in the channel. The drain current RTN characteristics of all devices as a function of time show themselves in the form of switching events between two states (not shown here). These switching events are attributed to trapping/detrapping caused by an individual interface defect close to the Si/ $SiO_2$ interface. The times in the high- and low-current states correspond to carrier capture and emission, respectively. The extracted mean capture time ($\tau_c$) and mean emission time constant ($\tau_e$) versus gate overdrive ($V_G - V_T$) are presented in Fig. 3. We can find that device C with thicker SMT film shows the lower values of $\tau_c$ and $\tau_e$, and the weak dependence of $\tau_e$ on gate voltage overdrive in nMOSFETs, indicating that the position of trap is closer to the Si/$SiO_2$ interface. This may result from the trap energy level near the channel conduction band in nMOSFETs with the higher tensile strain in the channel. Therefore, the electron can be captured or emitted more easily. Figure 4 shows the dependence of $\tau_c/\tau_e$ on gate overdrive for all devices. The $\tau_c/\tau_e$ ratio is dominated by the difference between conduction band ($E_C$) and trap energy ($E_T$). From the data obtained for $\ln(\tau_e)$ dependence on gate voltage, the position of the trap into the oxide ($x_t$) are determined using Eq. (1) following [6]

$$\frac{\partial \ln(\tau_e)}{\partial V_{GS}} = \frac{q}{KT}\left(\frac{x_t}{t_{ox}}\right)\left[1 - \frac{KT}{q}\frac{G_m}{|I_{DS}|}\right] \qquad (1)$$

where $t_{ox}$ is the oxide thickness, K is Boltzmann constant and $\tau_e$ is emission time. The extracted $x_t$ are 1.08 nm, 0.54 nm and 0.36 nm for device A, device B and device C, respectively. Moreover, less $x_t$ dependence on gate voltage was found in the thicker SMT film nMOSFETs. The mechanism underlying the smaller $x_t$ in the thicker SMT film device can be explained by the fact that the uniaxial tensile stress induces conduction band-offset and increases tunneling barrier height for electron ($\varphi_B$). The schematic energy band diagram for both devices is illustrated in Fig. 5. The observed gate tunneling current characteristics are used for the easy verification of $\varphi_B$ [7]. Figure 6 shows the gate current density (Jg) as a function of the gate voltage for all devices. Obviously, the smaller gate tunneling current density of the Device B (C) also confirms that the device has a higher $\varphi_B$ than the Device A. The higher $\varphi_B$ results in a reduction in tunneling attenuation length ($\lambda$) in the high uniaxial tensile stress device according to eq. 2 [7]

$$\lambda = \frac{h}{\sqrt{2\varphi_B m^*}} \qquad (2)$$

Moreover, the relation between the trap location $x_t$ and the tunneling attenuation length $\lambda$ can be given by equation $x_t = \lambda \ln(1 / 2\pi f \tau_0)$ [8] where the time constant $\tau_0$ is usually taken as $10^{-10}$ s. From this equation, trap depth is proportional to $\lambda$; therefore, the reduced $\lambda$ means that the higher uniaxial tensile device has a smaller depth in $SiO_2$ than the A device. On the other hand, temperature-dependence measurements enable the extraction of the energy barrier ($\Delta E_B$) for determining the carrier capture and the trap binding energy ($\triangle E_{CT} = E_C - E_T$) [9] of the defect. Equations (3) and (4) show the relation between temperature and mean capture (emission) time [5].

$$I_d(T)T^2\tau_c = \frac{\exp\left(\frac{\Delta E_B}{KT}\right)}{\sigma_0 \chi} \qquad (3)$$

$$T^2\tau_e = \frac{\exp\left(\frac{\Delta E_B + \Delta E_{CT}}{KT}\right)}{\sigma_0 g \eta} \qquad (4)$$

where $\sigma_0$, $\eta$, and $X$ are constants independent of temperature. Specifically, $\sigma_0$ physically represents the penetration of the wave function into the oxide and the increase in capture cross section will result in a smaller depth of traps from the $SiO_2$/Si interface. Figure 7 shows the temperature dependence of the RTN fluctuations for all devices. The capture and emission times decrease with the temperature increase. From the Fig. 7 data, we find the following Device A: $\Delta E_B = 0.09$ eV, $\sigma_0 = 1.02\times10^{-20}$ $cm^2$, and $\Delta E_{CT} = 0.21$ eV, Device B: $\Delta E_B = 0.12$ eV, $\sigma_0 = 1.7\times10^{-20}$ $cm^2$, and $\Delta E_{CT} = 0.15$ eV, Device C: $\Delta E_B = 0.15$ eV, $\sigma_0 = 3.54\times10^{-20}$ $cm^2$, and $\Delta E_{CT} = 0.08$ eV. On the other hand, the mean emission time constant is given by eq. (5) [9]. From Fig. 3, it is found that device C with thicker SMT film

has a smaller emission constant, which results from the smaller energy difference ($\Delta E_{CT} = E_C - E_T$).

$$\ln(\tau_e) = \ln\left(\frac{1}{\sigma v_{th} N_C}\right) + \frac{E_C - E_T}{kT} \qquad (5)$$

Using the above extracted results, a schematic configuration-coordinate diagram showing the changes in the total energy of the system as an electron is transferred from the inversion layer into an interface defect is shown in Fig. 8. Clearly, the larger $\sigma_0$ observed, the reduction in the trap binding energy $\Delta E_{CT}$, the shorter capture time and emission time for the strained devices than for the unstrained device all indicate that the trap location is closer to the $Si/SiO_2$ interface, which presents an intrinsic tensile strain-induced property.

## 4. Conclusion

In this paper, we present the impact of tensile strain induced by different SMT film thickness on oxide trap properties. Through RTN measurement, we found that the trap position of nMOSFETs with thick SMT film devices has shorter distance from $Si/SiO_2$ interface. This is because of the trap energy level near the channel conduction band in nMOSFETs with thick SMT film attributable to the higher tensile strain in the channel.


## Acknowledgements

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## References


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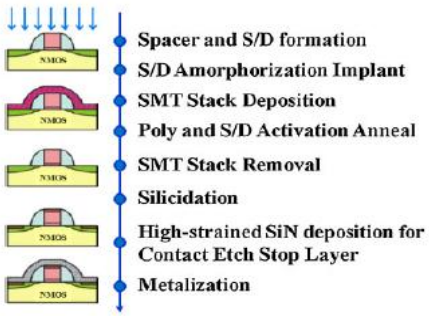


Fig. 1 Schematic of nMOSFET structure with process flow sequences for SMT process.

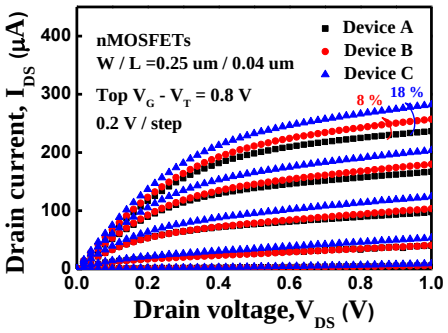


Fig. 2 The $I_{DS}$ - $V_{DS}$ characteristics for different SMT thickness nMOSFETs.

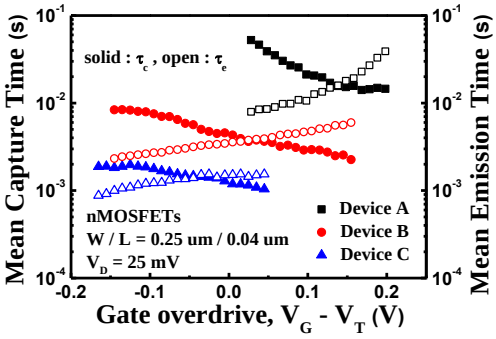


Fig. 3 Comparison of the capture time (solid) and emission time (open) for devices.

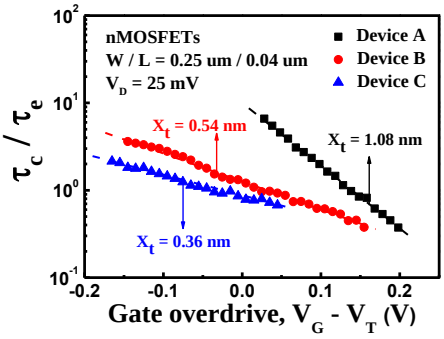


Fig. 4 Plot of capture time ($\tau_c$) over emission time ($\tau_e$) versus gate overdrive for the different SMT thickness nMOSFETs.

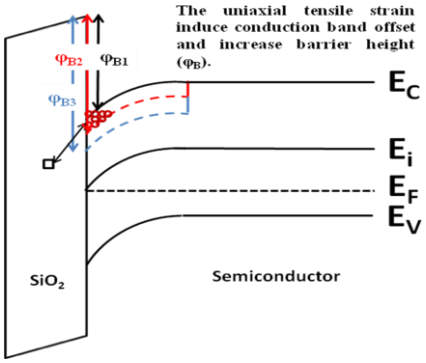


Fig. 5 Schematic energy band diagram for all devices. $\varphi_{B1}$, $\varphi_{B2}$ and $\varphi_{B3}$ indicate the barrier height for Device A, Device B, and Device C, respectively.

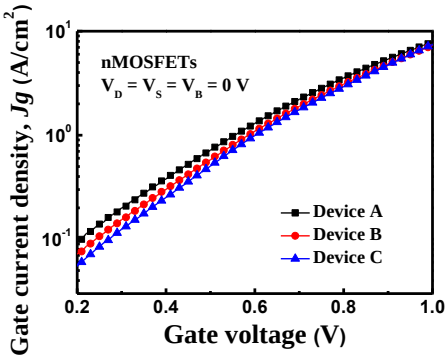


Fig. 6 Gate current density (*Jg*) as a function of gate voltage for all devices.

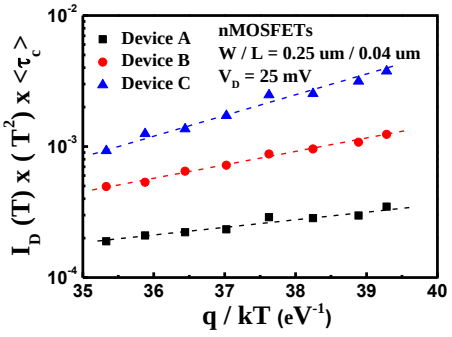


Fig. 7(a) Temperature dependence of mean capture time for all devices is shown.

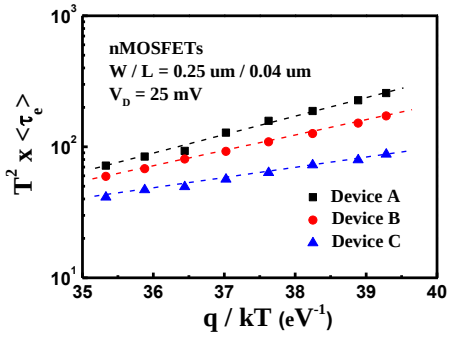


Fig. 7(b) Temperature dependence of mean emission time for all devices is shown.

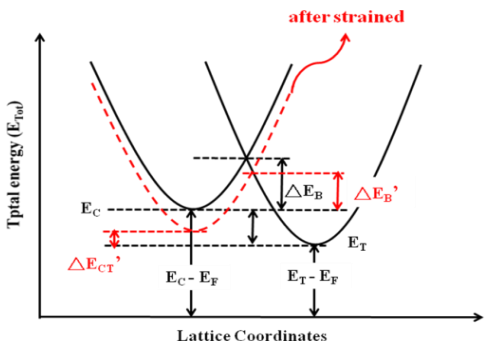


Fig. 8 Schematic configuration-coordinate diagram showing the changes in total energy of the system as electron is transferred from the inversion layer into an interface defect.