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1/f Noise Characteristic in Independent-Double-Gate-FinFET

Hideo Sakai[1], Shin-ichi O'uchi[2], Kazuhiko Endo[2], Takashi Matsukawa[2], Yongxun Liu[2],Yuki Ishikawa[2], Junichi Tsukada[2], Tadashi Nakagawa[2], Toshihiro Sekigawa[2], Hanpei Koike[2], Meishoku Masahara[2] and Hiroki Ishikuro[1]

[1]Department of Electronics and Electrical Engineering, Keio University.
3-14-1, Hiyoshi, Kohoku-ku, Yokohama 223-8522, Japan
Phone: +81-45-566-1443 E-mail: sakai@iskr.elec.keio.ac.jp
[2]National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan
AIST Tsukuba Central 2, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, Japan

1. Introduction

A FinFET (Fig. 1 (a)) is the most promising candidate to replace planer MOSFETs as the next generation transistor. Especially, the Independent-Double-Gate- (IDG-) FinFET (Fig. 1 (b)), whose double gates can be independently controlled, enables the new circuit technique such as ultra-low voltage OpAmps [1].

Device noise characterization becomes very important in analog circuit design. Especially the 1/*f* noise strongly depends on the channel condition. Since the channel condition of the IDG-FinFET has complex relation with the first and second gate voltages, V_{gs1} and V_{gs2}, it becomes important to study the 1/*f* noise at various operational conditions compared to that of the Common-Double-Gate- (CDG-) FinFET.

2. Device Structure and Measurement Setup

The measured IDG-FinFET has the following device parameters: the height (h_{fin}) and thickness (t_{fin}) of the Fin structure are 50 nm and 20 nm, respectively. Gate oxide thickness (t_{ox}) is 2.5 nm. The gate electrode was formed by TiN film covered by n^+ poly-Si [2]. Device with the gate length (L_g) 180 nm were fabricated. A cross-sectional TEM image of the fabricated FinFET is shown in Fig.2.

The measurement setup of the flicker noise is shown in Fig.3. Since the drain current (I_d) of the FinFET transistor with a single Fin channel is very small, the load resistance (R_L) should be large (> 10 kΩ) to obtain enough voltage gain. As a result, the frequency response of the measurement setup has low-pass characteristics with cutoff frequency around 10 kHz. To improve the accuracy of the 1/*f* noise measurement, this frequency response was compensated from the measured results.

3. Measurement Results

Fig.4 shows the I_d-V_{gs1} characteristic as the V_{gs2} is changed from -0.5 V to 1.0 V with 0.1 V step.

In the 1/*f* noise measurement two bias conditions were chosen. In the CDG mode (V_{gs1} = V_{gs2}), the conduction channel is formed at both Fin side-walls. In the IDG-mode (V_{gs1} = 0 or V_{gs2} = 0), the conduction channel is formed only at one side-wall of Fin. Fig.5 shows one example of the bias condition. To keep the current density I_d of the IDG mode (a) is kept half of that of IDG-mode (b). The frequency characteristic of the normalized S_{id} is shown in Fig.6.

The relation between the S_{id}/I_d^2 and I_d is shown in Fig.7. From the view point of circuit design, the S_{id}/I_d^2 of the IDG mode is normalized by the channel width because two Fin structures should be used in the IDG mode to obtain the same trans-conductance at same bias current. The figure shows that the normalized S_{id} is in inverse proportional to the I_d and almost the same in both the IDG- and CDG-modes if the current density is set at the same.

4. Discussion

The flicker noise (S_{id}) is in proportion to the product of I_d and the effective mobility, μ_{eff} [3]. μ_{eff} depends on the effective electric field ($\boldsymbol{E}_\perp$) in the channel. Fig. 8 shows the calculated relation between the $\boldsymbol{E}_\perp$, V_{gs1} and V_{gs2} with TCAD. It is compared to that calculated by using equations proposed in our previous work [4]. The solid line is the bias condition which keeps I_d at constant value. The black and dark gray lines are electric field of in the channel of gate1 and gate2, respectively. By using this result, the relation between S_{id}/I_d^2 and $\boldsymbol{E}_\perp$ can be obtained as shown in Fig. 9. In the same device, the S_{id}/I_d^2 decreases together with increasing $\boldsymbol{E}_\perp$. However, even with different strength of $\boldsymbol{E}_\perp$ in respect to IDG mode and CDG mode, the value of S_{id}/I_d^2 is almost the same, when I_d is the same. To obtain the same current density, $\boldsymbol{E}_\perp$ in the IDG mode should be higher than CDG mode. Therefore, μ_{eff} in the IDG-mode is lower than that of CDG mode. However, Fig.7 shows that S_{id}/I_d^2 was almost the same in both the CDG and IDG-modes if the current density was set at same value. This suggests that μ_{eff} or $\boldsymbol{E}_\perp$ has a minor effect on the flicker noise compared to I_d when the IDG- and CDG-FinFETs are used in analog circuits with overdrive voltage around 200 mV. It is noted that the flicker noise caused by the mobility fluctuation originates in the carrier scattering by oxide charges, while the on current is dominated by the phonon scattering or the surface roughness scattering [5]. This is consistent with the result that the flicker noise does not depend on the operation modes, IDG or CDG.

5. Conclusion

1/*f* noise of the IDG-FinFET was measured and compared to that of the CDG-FinFET. Based on the comparison of I_d-1/*f* noise characteristics of IDG- and CDG-FinFETs, it can be seen there is no significant difference in characteristic between both of them. It is possible to conclude that even by using the IDG mode, its 1/*f* noise performance does not deteriorate in comparison to CDG mode.

References

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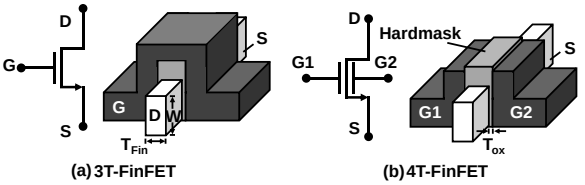

Fig.1 Schematic device strucutres of (a) Common-Double-Gate- (CDG-) FinFET and (b) Independent-Double-Gate- (IDG-) FinFET.

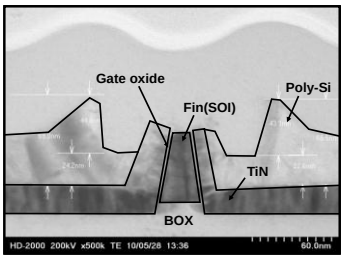

Fig.2 Cross-sectional TEM image of a fabricated IDG-FinFET.

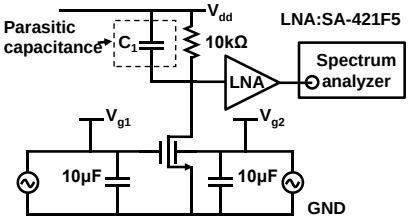

Fig.3 1/f noise measuring circuit configuration

To amplify the small FinFET signal, a resistor of 10kΩ is connected between the V_{dd} and drain terminal. The frequency characteristic of the measuring circuit is taken first to enable extraction of the 1/f noise characteristic by removing the C1' frequency characteristic embedded in the measuring result. A 10uF capacitor is connected between the gate terminal and GND to reduce of fluctuating gate voltage on the drain current.

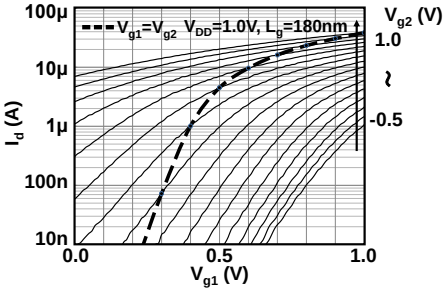

Fig.4 I_d-V_{g1} characteristics of the fabricated 4T-FinFET. V_{g2} is swept from -0.5V to 1.0V with 0.1-Vstep. I_d-V_g characteristic for V_{g1}=V_{g2} is marked with a line with symbols.

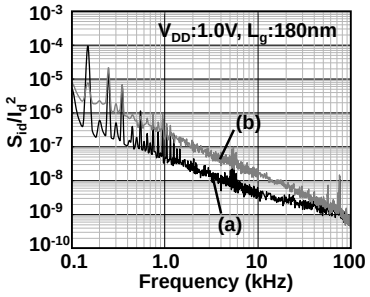

Fig.5 1/f Noise (Sid/Id2)-Frequency characteristics with operational modes of (a) V_{g1}=V_{g2} (CDG) at I_d=7.1μA (b) V_{g1}=0.8 V and V_{g2}=0V (IDG) at I_d=3.5uA

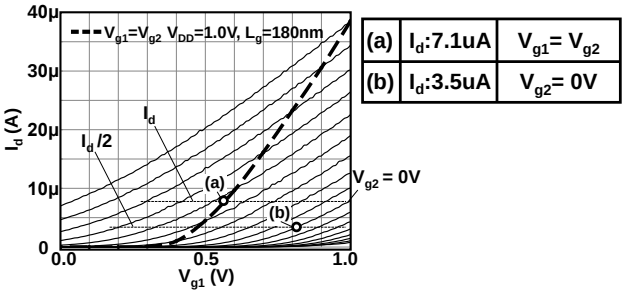

Fig.6 The bias condition shown in I_d-V_{g1} characteristics during 1/f Noise measurement: (a) CDG-mode bias condition; (b) IDG-mode bias condition.

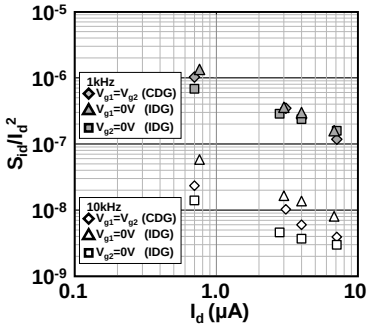

Fig.7 1/f Noise (S_{id}/I_d^2)-I_d Characteristic. The comparison of S_{id}/I_d^2 for CDG mode and IDG mode with a normalized current density in Fin Channel. Based on the above result, with fixed current density, the performance of S_{id}/I_d^2 for both CDG mode and IDG mode are almost the same.

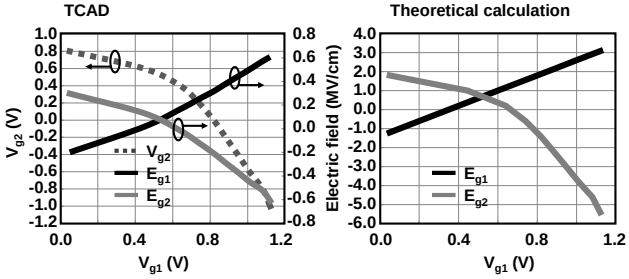

Fig.8 The comparison between TCAD and Theoretical Calculation of effective electric field. The left figure represent the TCAD result, and the right shows the calculation result. Both the TCAD and the calculation result shows proportional relationship.

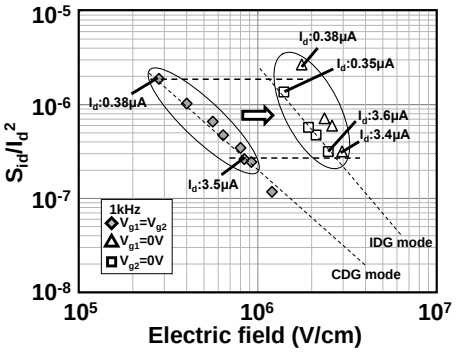

Fig.9 1/f Noise (S_{id}/I_d^2)-$E_\perp$ Characteristic. The non-colored marker represent CDG mode, while colored marker represent IDG mode. With equal exerted up the Fin, the CDG mode have shown noise reducing trend than the IDG mode.