

Narrow Width Effects on High Frequency Performance and RF Noise of Sub-40nm Multi-finger nMOSFETs

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Abstract

The impact of narrow width effects on high frequency performance parameters like f_T , f_{MAX} , and RF noise in 35 nm multi-finger n-MOSFETs is investigated in this paper. Multi-OD devices with reduced width under fixed finger number (N_F) lead to higher R_g and suffer the penalty in f_T , f_{MAX} , and NF_{min} . On the other hand, narrow-OD MOSFET with larger N_F can yield lower R_g and higher f_{MAX} . However, these narrow-OD devices even with lower R_g suffer lower f_T and higher NF_{min} . The mechanisms responsible for narrow width effects on f_T , f_{MAX} , and noise parameters will be presented to offer an important guideline of MOSFET layout for RF circuits design using nanoscale CMOS technology.

I. Introduction

Nanoscale CMOS devices with multi-finger layout have been extensively used for higher f_T and f_{MAX} , and lower RF noise driven by gate length scaling and gate resistance (R_g) reduction from multi-finger structure [1-3]. Unfortunately, the continuous reduction of finger width (W_F) and increase of finger number (N_F) for smaller R_g may lead to the penalty of lower transconductance (g_m) and larger parasitic capacitances. The former one comes from stress induced mobility degradation and the latter one stems from gate related fringing capacitances [4-5]. Both can not be scalable with device scaling and the impact may dominate high frequency characteristics in nanoscale devices. The potential impact from parasitic capacitances and the trade-off with R_g becomes a critical factor governing the specified RF performance parameters and has to be considered seriously in devices layout for RF circuit design.

II. Experimental

The multi-finger n-MOSFETs were fabricated in 65nm CMOS process, with 35nm physical gate length and the total gate width fixed at 64 μm ($W_{tot}=W_F \times N_F=64\mu m$). Fig.1(a)~(c) illustrate multi-finger MOSFET layouts, namely standard, narrow-OD, and multi-OD devices in which $\sigma_{//}$ and σ_{\perp} denote the longitudinal and transverse stresses introduced from STI. S-parameters were measured by Agilent network analyzer E8364B up to 40GHz. In particular, open and short deembedding to the bottom metal, i.e. M1, were performed to remove the parasitic capacitances from the pads as well as interconnection lines [5]. Four noise parameters, such as NF_{min} , R_n , $Re(Y_{opt})$, and $Im(Y_{opt})$ can be measured by using ATN-NP5B from 1GHz up to 18GHz.

III. Results and Discussion

Fig. 2(a) demonstrates g_m versus V_{GT} ($V_{GS}-V_T$) in saturation region measured from narrow-OD and standard nMOS. This monotonic degradation of g_m with W_F scaling suggests that the increase of compressive σ_{\perp} is the dominant factor responsible for mobility degradation and the resulted g_m reduction [6]. As for multi-OD nMOS shown in Fig. 2(b), the $g_{m,max}$ of OD4 and OD8 are degraded by 11.2% and 18.9%, as compared to OD1, but the degradation becomes smaller to 8.5% for OD16. According to our recent work [7], the increase of effective width (W_{eff}) from STI top corner rounding induced ΔW can compensate mobility degradation. Note that ΔW of nMOS in this process is 38.7 nm. With the

increase of N_{OD} , ΔW effect will be enhanced and may dominate STI σ_{\perp} effect, which explain the increase of g_m when scaling W_{OD} from 0.25 μm for OD8 to 0.125 μm for OD16. Fig. 3(a) reveals that W_F scaling in narrow-OD nMOS leads to a monotonic f_T degradation. An analytical model given by (1) [8] suggests that f_T degradation can be originated from g_m degradation and/or increase of C_{gg} . For narrow-OD nMOS, the smallest g_m appearing in W05N128 (Fig.2(a)) is considered as one of major factors responsible for the worst f_T . Furthermore, the measured C_{gg} (Fig.3(b)) indicates 8.3% increase of C_{gg} in W05N128. The combined effect from lower g_m and larger C_{gg} can explain f_T degradation in narrow-OD devices [5]. As for multi-OD nMOS, Fig.4(a) again indicates a monotonic degradation of f_T with W_{OD} scaling. Obviously, OD16 with the smallest width (0.125 μm) suffers the lowest f_T . As shown in Fig.4(b), OD16 reveals substantially larger C_{gg} compared to OD1. Although OD16 yields higher g_m than OD4 and OD8, due to ΔW effect (Fig.2(b)), the much larger C_{gg} offsets the g_m increase and leads to f_T degradation.

Fig. 5(a) presents an increase of f_{MAX} with W_F scaling and the highest f_{MAX} achieved by W05N128. The f_{MAX} can be calculated by (2) [8], which indicates that the higher f_T and lower R_g can enhance f_{MAX} . Referring to Fig.3(a), W05N128 suffers the lowest f_T . However, the smaller W_F and larger N_F in narrow-OD devices can reduce R_g as shown in Fig.5(b). Almost 50% lower R_g realized by W05N128 can over-compensate f_T degradation and contribute to higher f_{MAX} . On the other hand, multi-OD nMOS shown in Fig.6(a) indicates a monotonic degradation of f_{MAX} with W_{OD} scaling. Referring to Fig.4(a), the larger N_{OD} , i.e. the smaller W_{OD} indeed leads to f_T degradation. As for R_g shown in Fig.6(b), the smaller W_{OD} (larger N_{OD} and fixed N_F) suffers the higher R_g and OD16 reveals around 20~25% higher R_g . According to (2), the lower f_T and larger R_g appearing in multi-OD devices are two key factors responsible for f_{MAX} degradation with W_{OD} scaling.

Fig. 7(a)-(d) present NF_{min} , R_n , $Re(Y_{opt})$, and $Im(Y_{opt})$ measured from the standard and narrow-OD nMOS (1~18GHz). W05N128 with the smallest W_F and R_g suffers 0.2~0.5dB higher NF_{min} in 9~18GHz. Fig.7(c) and (d) reveal significant increase of $Re(Y_{opt})$ and $Im(Y_{opt})$ (absolute value) in W05N128 at higher frequencies, above 9GHz. According to (3)~(4) [8], the increase of either R_n or $Re(Y_{opt})$ will result in higher NF_{min} and the calculated NF_{min} can fit measured data in terms of frequency and layout dependence as shown in Fig.7(a). This proven model combined with Fig.7(b) and (c) for measured R_n and $Re(Y_{opt})$ indicates that the increase of $Re(Y_{opt})$ is the primary factor responsible for higher NF_{min} in narrow-OD nMOS. According to (5) for R_n , the benefit of smaller R_g in narrow-OD device happens to be cancelled out by the increase of the second term due to lower g_m from compressive σ_{\perp} . As for multi-OD nMOS shown in Fig.8(a)-(d), OD16 reveals the largest value in $Re(Y_{opt})$ and $Im(Y_{opt})$, leaving R_n as the exception. It is interesting to note that OD16 suffers the largest R_g (Fig.6(b)) but achieves R_n lower than OD8. Referring to (5), the higher g_m can help reduce R_n , due to smaller g_{do}/g_m^2 , and reverse the correlation between R_n and R_g . It explains why OD16 has the larger R_g but smaller R_n than OD8. The counterbalance between $Re(Y_{opt})$ and R_n results in comparable NF_{min} between OD16 and OD8. All of multi-OD nMOS suffer higher NF_{min} than OD1.

$$f_T = \frac{g_m}{2\pi\sqrt{C_{gg}^2 - C_{gd}^2}} \quad (1)$$

$$f_{MAX} = \frac{f_T}{2\sqrt{R_g(g_{ds} + 2\pi f_T C_{gd}) + g_{ds}(R_i + R_s)}} \quad (2)$$

$$F_{min} = 1 + 2R_n \text{Re}(Y_{opt})[1 + R_n \text{Re}(Y_{opt})] \quad (3)$$

$$NF_{min} = 10 \cdot \log F_{min} \quad (4)$$

$$R_n \approx R_g + \gamma \frac{g_{do}}{g_m^2} \quad (\gamma > 1 \text{ for short channel devices}) \quad (5)$$

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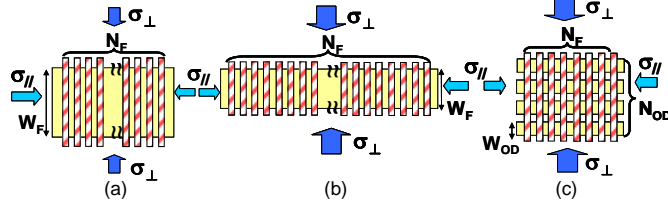


Fig. 1 Multi-finger MOSFET layouts with various W_F and N_F and STI stresses $\sigma_{//}$ and σ_{\perp} (a) standard device: $W_F \times N_F = 2\mu\text{m} \times 32$ (W2N32), (b) narrow-OD devices: $W_F \times N_F = 1\mu\text{m} \times 64$ (W1N64), $0.5\mu\text{m} \times 128$ (W05N128), and (c) multi-OD devices $W_{OD} \times N_{OD} = W_F = 2\mu\text{m}$: OD4, OD8, OD16.

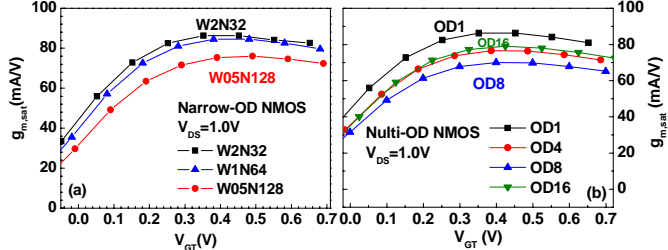


Fig. 2 The g_m versus V_{GT} ($V_{DS}=1V$) measured from (a) narrow-OD nMOS and (b) multi-OD nMOS. $g_m = \text{Re}(Y_{21})$ after open and short deembedding.

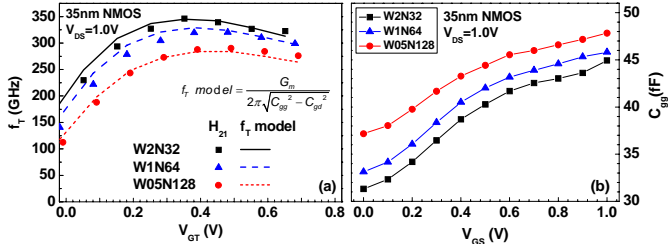


Fig. 3 (a) The measured and calculated f_T versus V_{GT} ($V_{DS}= 1.0V$) and (b) the gate capacitances C_{gg} versus V_{GS} extracted from $\text{Im}(Y_{11})$ for narrow-OD and standard nMOS

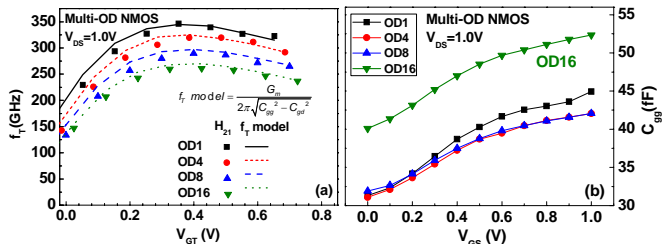


Fig. 4 (a) Measured and calculated f_T vs. V_{GS} ($V_{DS}=1.0V$) (b) C_{gg} vs. V_{GS} extracted from $\text{Im}(Y_{11})$ for multi-OD and standard nMOS.

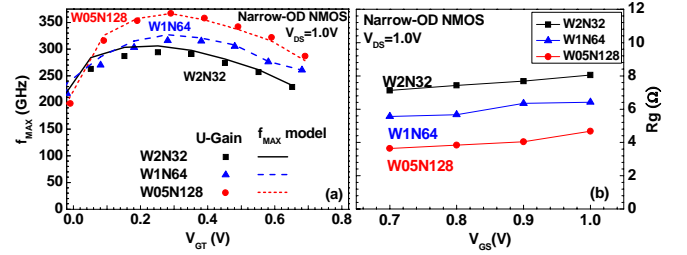


Fig. 5 (a) The measured and calculated f_{MAX} versus V_{GT} ($V_{DS}= 1.0V$) and (b) R_g versus V_{GS} for narrow-OD nMOS (W1N64, W05N128) and W2N32

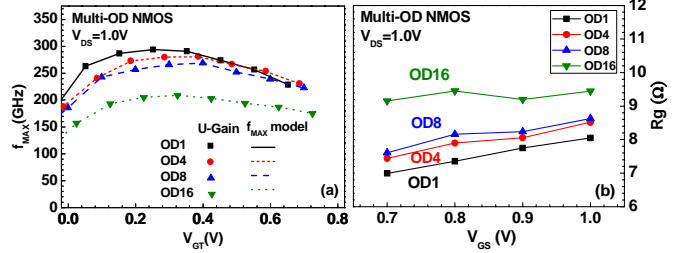


Fig. 6 (a) The measured and calculated f_{MAX} versus V_{GT} ($V_{DS}= 1.0V$) and (b) R_g versus V_{GS} for multi-OD nMOS (OD4, OD8, OD16) and OD1

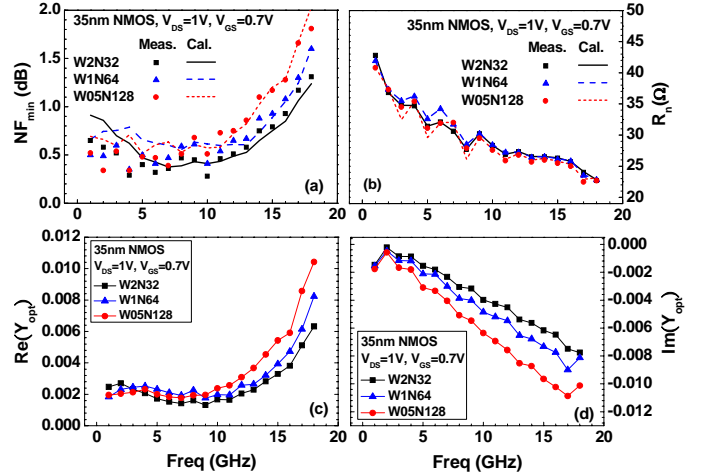


Fig. 7 Noise parameters of narrow-OD nMOS (a) measured and calculated NF_{min} (b) measured and calculated R_n (c) $\text{Re}(Y_{opt})$ (d) $\text{Im}(Y_{opt})$.

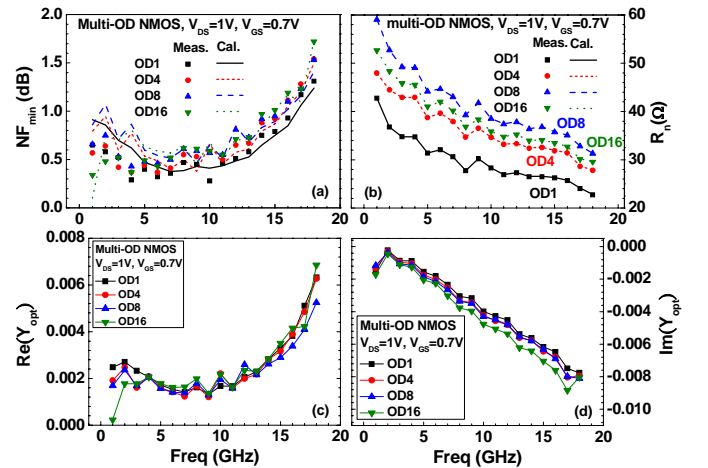


Fig. 8 Noise parameters of multi-OD nMOS (a) measured and calculated NF_{min} (b) measured and calculated R_n (c) $\text{Re}(Y_{opt})$ (d) $\text{Im}(Y_{opt})$.