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Lifetime evaluation on AC stress in High-K / Metal-Gate with Using Dual-Pulsed-Test-System (DPTS)

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1. Introduction

Lifetime under AC operation is generally gotten with the calculation from the DC degradation test result. The recovery effect is not usually considered at the operation condition. It became to be widely known that the degradation recovery occurs under the AC operation [1]. Therefore, in this study, we have investigated the recovery effect in AC operation. We have prepared the measurement system, which can apply AC voltage to gate and drain, respectively. The each effect for AC operation to lifetime has investigated.

2. Dual-Pulsed-Test-System (DPTS)

Dual-Pulsed-Test-System (DPTS) is able to apply a pulsed voltage to gate and drain, independently, as shown in Fig. 1. The gate and the drain are connected to the Function-Generators (FGs), respectively. The source and the substrate are connected to the Source-Measure-Units (SMUs), respectively. We have evaluated degradation rate of the transistor with observing source current (I_{SD}). We have investigated lifetimes of DC and AC stresses with using DPTS.

Test devices are PMOS transistor fabricated with high-k / Metal gate process. The transistor channel length / width are 0.027 um / 3 um.

The DC stress which is -1.4V of gate and drain voltage means Hot-Carrier-Injection (HCI) stress. The AC stress corresponds with operation of an actual inverter circuit. The AC pulses which applied to the gate and the drain are trapezoidal pulses, have 100 kHz of frequency, 150ns of rise and fall time, 0V of base voltage, and -1.4V of pulse height.

Figure 2 shows the degradation rate of I_{SD} under the DC stress and the AC stress, and the degradation rate of I_{SD} under AC stress that calculated from the DC stress. The experimental AC lifetime is about 10 times longer than the calculated AC lifetime.

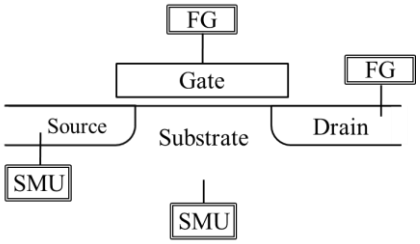

Fig. 1 Outline of Dual-Pulsed-Test-System (DPTS). The gate and the drain are connected to Function-Generators (FGs) respectively. The source and the substrate are connected to Source-Measure-Units (SMUs).

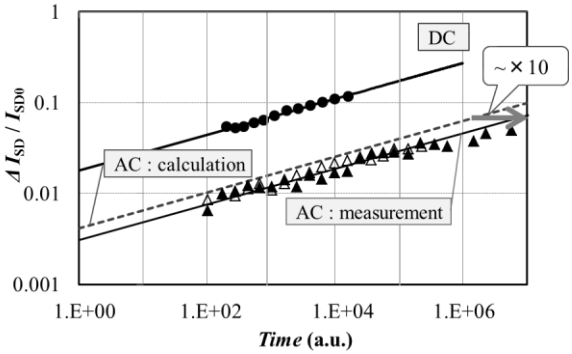

Fig. 2 Comparison of DC HCI and AC test and calculated line from DC. The experimental AC lifetime is about one order of magnitude longer than calculated one.

3. Lifetime evaluation on AC condition

For investigating the difference between the measured and the calculated lifetime, we have evaluated lifetimes under AC stress with the condition shown in Table I with using DPTS. The applied pulses to the gate and the drain by FGs are same with the AC stress test in session 2. The test temperature is 95 degrees centigrade. In Test I, -1.4V DC and AC stresses are applied to the gate and the drain respectively. In Test II, AC stress and 0V DC are applied to the gate and the drain. Test II correspond to AC-NBTI stress test. Test III, AC stress and -1.4V DC are applied to the gate and the drain. In addition, we have varied the duty of pulse for investigating the AC effect.

Table I Test Conditions

	Gate	Drain
Test I	DC(-1.4V)	AC
Test II	AC	DC(0V)
Test III	AC	DC(-1.4V)

Figure 3 shows the lifetime of Test I, II, and III as shown in Table I. The vertical axis shows the lifetimes, which is calculated the summation of the on-time of stress, and are normalized by the lifetime of 100% duty stress (DC stress).

The duty factor hardly affects the lifetime in Test I, however it affects strongly to the lifetime in Test II and III as shown in Fig. 3. This result shows that gate voltage cycle, not drain voltage cycle, contribute to the lifetime. The results indicate that NBTI recovery effect has appeared in Test II and III. Dependence of the duty on Test III is more sensitive than test II.

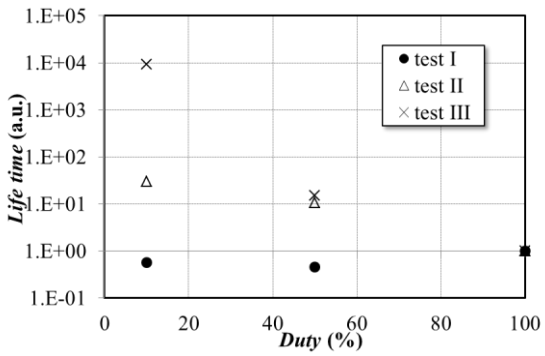

Fig. 3 Correlation between lifetime and duty cycle for different test condition. The lifetimes were normalized with the time of duty cycle = 100 %. Though there is little duty cycle dependence in gate DC / drain AC condition (Test I), the lifetimes become long with small duty (Test II, III).

We have evaluated drain current (I_D) and gate current (I_G), with varying gate voltage (V_G) at -1.4V of drain voltage (V_D) for investigating the difference between Test II and III. Electron current is dominant in I_G of more than around -0.7V and, hole current is dominant in I_G of less than around -0.7V as shown in Fig. 4.

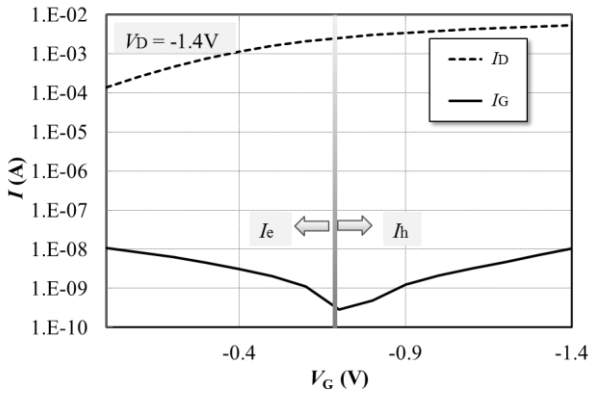

Fig. 4 Transistor characteristic at V_D = -1.4V. The I_G changes the polarity around V_G = -0.7V.

We have measured lifetimes with varying the pulse base voltage applied to the gate (V_{GPB}) from -0.4V to 0V (Fig. 5) on Test III of DPTS. Contribution to lifetime of -0.4V of V_G, i.e. V_{GPB}, is smaller comparing with of -1.4V. Time of V_{GPB} of -0.4V does not contribute to lifetime considering from DC test results. However, the lifetimes have changed with varying the V_{GPB} in the test as shown in Fig. 6.

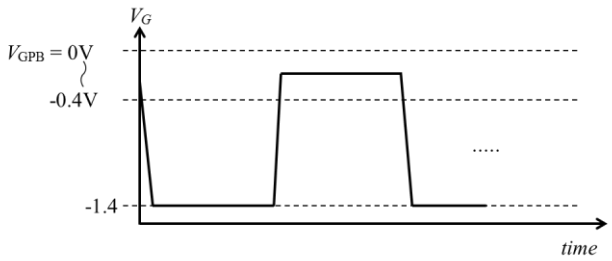

Fig. 5 The V_{GPB} were varied from -0.4V to 0V.

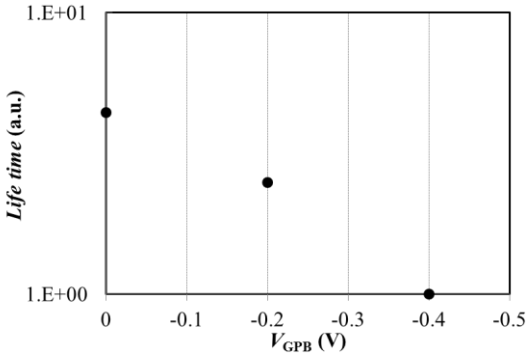

Fig. 6 Correlation between the V_{GPB} and the lifetime.

Figure 7 shows the lifetime as a function of I_G. The lifetime increases with increasing of I_G. Electronic injection to the gate accelerates recoveries. Higher V_{GPB} accelerates recovery due to increasing electron current like Test III (V_{GPB} is 0V).

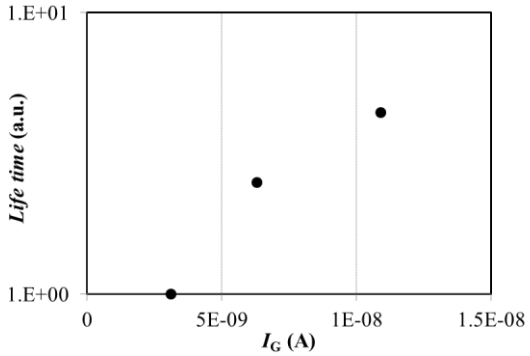

Fig. 7 Correlation between the I_G and the lifetime. The lifetime increases with increasing electron injection.

3. Conclusions

As for the recovery phenomenon in the AC operation, we find that voltage cycle of the gate is a key factor. In addition, it has been found that the effect of the recovery changes according to the shape of AC waveform. When the recovery effect is taken into the lifetime estimation of a real circuit, it is necessary to consider the above effect.

References

[1] S. Ramey, C. Prasad, M. Agostinelli, S. Pae, S. Walstra, S. Gupta and J. Hicks, *Proceedings of the Int. Reliability Physics Symp.*, (2009) 1023.

[2] Y. Wang, Solid-State Electronics **52** (2008) 264.