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Enhanced Subthreshold and Output Characteristics in Tunnel Field -Effect Transistors Using Shallow Junction Technologies

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1. Introduction

As MOSFETs scale, lowering power consumption is an important concern. Reducing the off-state leakage and scaling the supply voltage (V_{DD}) are the key steps, which mean the steep subthreshold swing (SS) [1]. It has been reported that Tunnel FET (TFET) can obtain a subthreshold swing smaller than 60mV/dec [2-3]. However, the steep subthreshold swing in the low current level and the small on-current limit its application in low power and high performance devices.

To improve carrier tunneling, getting a sharp lateral source doping profile in TFET is important [3-4]. In this study, a Si n-i-p TFET fabricated by plasma implantation and laser annealing are investigated for improving carrier tunneling. Si n-i-p TFETs fabricated by plasma implantation and different annealing schemes, laser annealing (LA) and rapid thermal annealing (RTA), were also characterized and discussed

2. Device Simulation and Fabrication

To understand the relationship between lateral source doping and TFET performance, Si n-i-p TFET with different lateral n^+ doping profiles at source side are simulated. Fig. 1 (a) shows the simulated structure of Si n-i-p TFET. Device simulation uses ISE-TCADs DESSIS [5] device simulator. Fig. 1 (b) presents the band diagrams of Si n-i-p TFETs with different lateral source doping profiles. The sharpest lateral doping profile, the box profile, has the smallest tunneling distance and enhanced lateral electric field across the tunneling path.

Fig. 2 illustrates parts of process flow of Si TFET with source pocket on the SOI substrate (T_{Si}=50nm). After the definition of SiN dummy gate and p^+ drain implantation, the device was covered with half mask on the drain area for low energy n^+ (AsH_3, 0^o, 2keV, 1e15cm^{-2}) plasma implantation and deep source implantation. Subsequently, LTO was deposited and laser annealing with 350mJ/cm^2 was used to activate the dopant. Then device is finished at replaced gate stack with high k (Al_2O_3, EOT=3.5nm)/metal gate and standard backend process.

3. Results and Discussion

Fig. 3 shows subthreshold characteristics of Si n-i-p TFETs (Lg=1μm) fabricated by plasma implantation and different annealing methods (LA with 350mJ/cm^2 and RTA with 1050 ^{o}C and 1 sec duration time). The I_{ON}/I_{OFF} ratio in TFET fabricated by LA ($6x10^6$) is 2 orders larger than TFET fabricated by RTA at V_{DS} = -1.1V. This result is expected since TFET fabricated by LA has a sharper n^+ source doping profile than TFET fabricated by RTA. As the tunneling probability is an exponential function of the tunneling distance [6], the small tunneling distance can induce more tunneling carriers.

Fig. 4 shows the output characteristics of Si n-i-p TFETs fabricated by plasma implantation and different annealing methods. TFET fabricated by LA exhibits higher saturation currents than TFET fabricated by RTA. At linear region of I_D-V_D curve, TFET fabricated by RTA shows a significant voltage drop, which relates to the existence of tunneling resistance in the device [7]. However, there is no obvious voltage drop in TFET fabricated with LA, which means reduced tunneling resistance in the device. TFET fabricated by LA has sharper lateral doping profile than TFET fabricated by RTA.

Fig. 5 shows the subthreshold characteristics of TFET fabricated by plasma implantation and LA at different temperatures. The small temperature-dependent subthreshold characteristics between 200 to 300K is due to trap-assisted tunneling. However, the temperature- dependent subthreshold characteristics become insignificant as the temperature is decreased below 200K. This proves the transport mechanism is dominated by band-to-band carrier tunneling.

Table 1 shows different technologies used to obtain sharp lateral source doping profile in Si TFETs. Si TFET with plasma implantation and laser annealing can get enhanced on-current and steep average subthreshold swing across the same current range.

4. Conclusion

Si n-i-p tunnel FET with sharp lateral n^+ source doping profile at source side is fabricated by plasma implantation and laser annealing. This method can be effectively applied in current CMOS technology for the low power devices.

References

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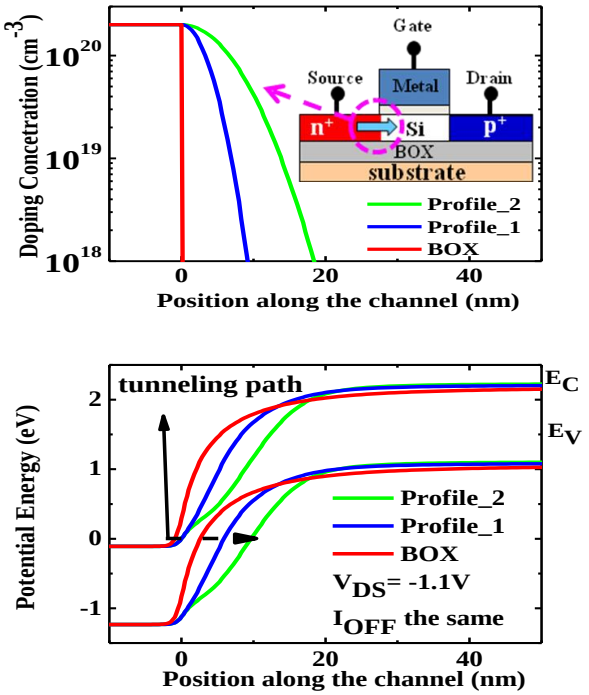

Fig. 1 (a) The device structure of Si n-i-p TFET with different lateral n^+ source doping profiles. (Lg=100nm, EOT=1nm, channel doping=1e16cm^{-3}, T_{Si}=50nm) (b) Simulated band diagrams of TFETs with different lateral source doping profiles.

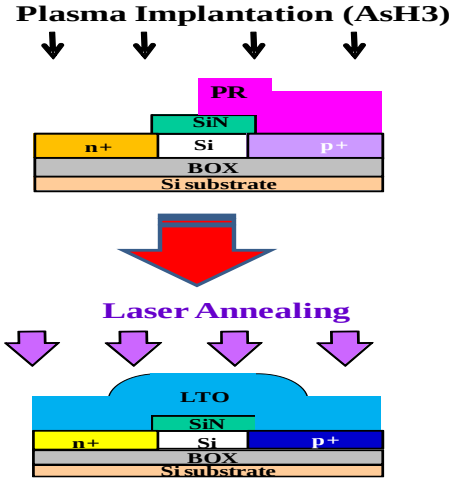

Fig. 2 Parts of process flow of TFET fabricated with laser annealing.

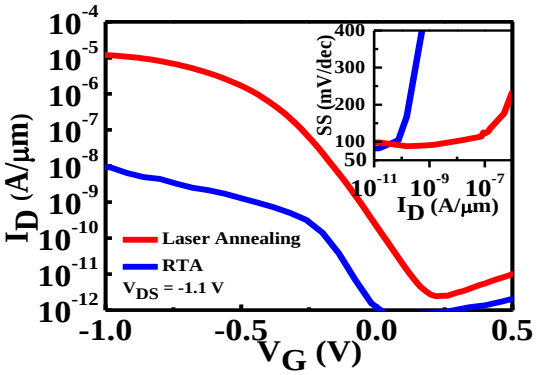

Fig. 3 The subthreshold characteristics of Si TFETs fabricated by plasma implantation and different annealing methods.

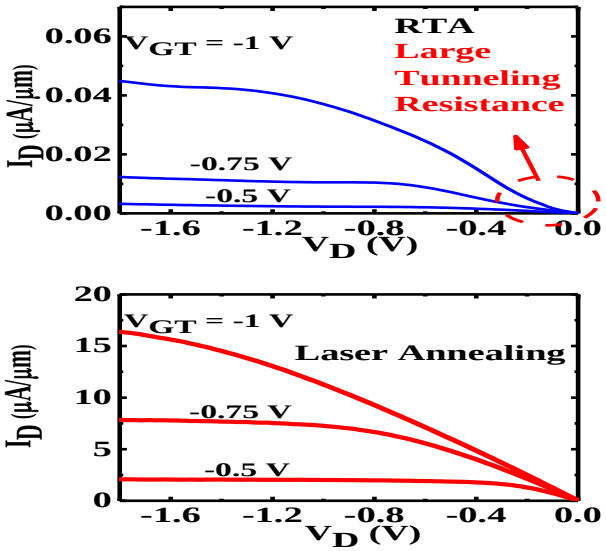

Fig. 4 The I_D-V_D curve of TFETs fabricated by (a) RTA and (b) laser annealing.

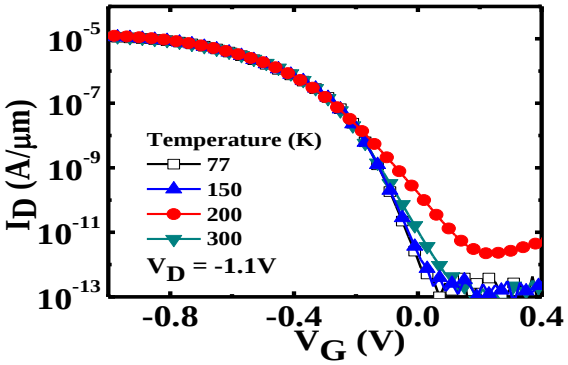

Fig.5 I_D-V_G curves of TFET fabricated by plasma implantation and laser annealing at different temperatures. (The curve shift with temperature has been accounted by shifting the curve to same V_G at 10^{-7}A/μm)

Table I.

	MBE [4]	Silicide Access [3]	**This work**
SS @ 1nA/um (mV/dec)	540	70	**90**
SS @ 0.1μA/um (mV/dec)	1000	260	**123**
I_{ON} [1] (μA/um)	0.03	1.2	**10**
I_{ON}/I_{OFF}	3x10^3	7x10^7	**5x10^6**

[1] $|V_{DS}| = |V_{GS}-V_{BTBT}| = 1.0$V.