Study of Off-State Breakdown Improvement and Hot-Carrier Reliability in LDMOS Device with Gradual Junction Structure

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1. Introduction

Both off-state breakdown voltage (V_{BD}) and on-resistance (Ron) performances are the major considerations in designing LDMOS devices. However, these two parameters are usually trade-off with each other. In this work, a gradual junction structure is used to improve off-state V_{BD} without sacrificing device drivability. Experimental data of V_{BD} improvement and hot-carrier induced device degradation are presented and discussed. In addition, TCAD simulation results of electric field and impact ionization (I-I) rate are analyzed to explain the experimental data. Finally, electrical safe operating area (E-SOA) of devices is investigated. The device with gradual junction structure has wider E-SOA range.

2. Experiment

The dimensions of W/L and gate oxide thickness of the device used in this work are 10/0.9 \textmu m and 40 nm, respectively. Fig. 1(a) and (b) show the schematic process flows to fabricate LDMOS device with traditional and gradual junction structures, where the self-alignment implant of N\textsuperscript{-} region experience uniform and gradual screen oxide thickness. The gradual screen oxide structure, which is formed by dual oxide (8nm and 40nm) process, leads to gradual junction profile in N\textsuperscript{-} region of LDMOS device. After self-alignment implant of N\textsuperscript{-} region, a n\textsuperscript{+} implant with a distance 0.75 \textmu m to the poly gate is defined.

(a) LDMOS with traditional LDD
(b) LDMOS with gradual LDD

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(a) & (b) \\
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N\textsuperscript{+} implant to poly gate offset & N\textsuperscript{+} implant to poly gate offset \\
N- implant & N- implant \\
N\textsuperscript{+} poly gate & N\textsuperscript{+} poly gate \\
Thick oxide & Thin oxide \\
P-well & N- \\
N\textsuperscript{+} implant to poly gate offset & N\textsuperscript{+} implant to poly gate offset \\
N- implant & N- implant \\
N\textsuperscript{+} poly gate & N\textsuperscript{+} poly gate \\
Thick oxide & Thin oxide \\
P-well & N- \\
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Fig. 1 (a) and (b), the schematic process flows to fabricate traditional and gradual junction structures are compared.

3. Experiment Results and Discussions

Fig. 2 shows the off-state breakdown characteristics for devices with traditional and gradual junction profile. Compared with the device with traditional structure, the device with gradual junction profile has better V_{BD} which is improved by about 1V. This improvement can be explained by TCAD simulation results in Fig. 2. At the same drain voltage (V_D), the device with gradual junction profile has smaller electrical field (~3.4\%) in outline A-A” than the device with traditional structure, leading to improved V_{BD}.

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Fig. 2, Comparison of V_{BD} data and E-field simulation results.

Fig. 3 shows substrate current (I_{SUB}) vs. gate voltage (V_G) characteristics under V_D = 12V, 13V, and 14V. At V_G is roughly 3V, the value of first I_{SUB} peak is about the same between devices with traditional and gradual junction profile. As the V_G is greater than roughly 6V, Kirk effect is becoming significant and I_{SUB} rises again. Such Kirk effect induced I_{SUB} rise is less severe in the device with gradual junction profile. The suppression of Kirk effect can be explained by TCAD simulation results. As seen in Fig. 3, at V_D = 14V and V_G = 7V, the device with gradual junction profile has smaller I-I rate, leading to smaller I_{SUB}.

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Fig. 3, Comparison of I_{SUB} data and impact ionization simulation results.
Since the device with gradual junction profile can suppress Kirk effect and leads to smaller $I_{SUB}$ at high $V_G$ bias, hot-carrier reliability of this device is likely to be improved. Fig. 4 shows the device parameter degradation of two kinds of device under 5000s of hot-carrier stress. The device parameters monitored are Ron and drivability current ($I_{DTot}$) which are measured at $V_D = 0.1V$ and $V_D = 8V$, respectively. For devices stressed under the same $V_D$ and $V_G$ ($V_D = 14V$, $V_G = 6V$), the device with gradual junction profile shows smaller Ron and $I_{DTot}$ degradation. This result suggests that reduced $I_{SUB}$ (under the same $V_G$) caused by suppression of I-I rate improves hot-carrier reliability. In order to realize the relation between $I_{SUB}$ and device degradation, Fig. 4 also shows the amount of device degradation under 5000s stress for devices stressed at $V_G$ bias (6V, 7V, and 7.5V) such that $I_{SUB}$ rise caused by Kirk effect is significant. Stress data show that for devices stressed under the same $I_{SUB}$, the device with gradual junction profile produces more device degradation than the device with traditional structure. Remember that higher $V_G$ bias is needed for the device with gradual junction profile to produce the same $I_{SUB}$ (due to the suppression of Kirk effect). Thus, higher $V_G$ results in more electron injection to the gate oxide, leading to more device degradation [2].

![Fig. 4](image)

Fig. 4, Comparison of device degradation data under hot-carrier stress.

Finally, the E-SOA of devices with traditional and gradual junction structures is investigated. Fig. 5(a) depicts the measurement setting to obtain E-SOA, where different $V_G$ steps and 100ns pulse of $V_D$ are applied to the device. The breakdown points are judged at a given $V_G$ and pulsed $V_D$ which causes device burned. Results in Fig. 5(b) reveal that the device with gradual junction profile has wider E-SOA range than the device with traditional structure. Improvement of E-SOA range is suggested to be caused by suppression of $I_{SUB}$ and better latch-up behavior.

![Fig. 5(a)](image)

**Fig. 5(a)**: Vg steps: 3.5 to 10V

![Fig. 5(b)](image)

**Fig. 5(b)**: Constant Vg, 100ns pulse for Vd, Vs=Vb=0V

**Fig. 5**: the measurement setting and comparison of electrical safe operation area (E-SOA) data.

### 3. Conclusions

A simple mask modification which produces gradual screen oxide structure can be utilized to fabricate LDMOS devices with gradual junction profile in the N- region. In off-state operation, the device with gradual junction structure shows roughly 1V improvement in $V_{BD}$ due to suppression of electrical field. In on-state operation, the device with gradual junction structure has less Kirk effect induced $I_{SUB}$ rise due to suppression of I-I rate. For hot-carrier stress under the same $V_G$ bias, the device with gradual junction structure exhibits less device parameter degradation due to suppression of I-I rate. For hot-carrier stress under the same $I_{SUB}$, however, the device with gradual junction structure produces worse device degradation. The reason responsible for this phenomenon is that higher $V_G$ is needed to produce the same $I_{SUB}$ leading to more electron injection to the gate oxide. Finally, experimental data show that the device with gradual junction structure has wider E-SOA range than the device with traditional structure.

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### References
