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Investigation of P/NBTI in High-κ Gate Dielectric MOSFETs by Id-RTS

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1. Introduction

Positive and negative bias temperature instability (P/NBTI) has been recognized as two major reliability issues in advanced CMOSFET systems containing MG/HK dielectrics [1]. On the other hand, one of the most significant reliability issues in advance device scaling is random telegraph signal (RTS) [2~4]. Recent studies have shown charging/discharging of oxide defects induce threshold voltage amplitude distribution in RTS and NBTI [5]. We are focused on current fluctuations in high-κ (HfO_2) gate dielectric MOSFETs due to RTS amplitude distribution under positive and negative bias temperature instability (P/NBTI). By using the statistical analysis after a long term and high temperature test, the lifetime with Id-RTS can be estimated by graphical extrapolation, which helps intuitive understanding of RTS impact on the reliability of high-κ/metal gate reflect the ultimate ability of circuit design.

2. Experiment

RTS measurement in high-κ (HfO_2) gate dielectric and metal gate MOSFETs are performed with fast and accurate I-V characterization using Agilent B1530A. The n- and p-MOSFETs have a drawn gate length of 0.03 um and a gate width of 0.75 um, respectively. The effective oxide thickness of HK dielectrics in n-MOSFET is 1.18 nm and in p-MOSFET is 1.16 nm, respectively. Fig. 1 shows Id fluctuation due to charge trapping/de-trapping in the oxide. The complex RTS is observed both for n- and p-MOSFETs as shown in Figs.2 (a) and (b), respectively.

3. Results and Discussion

The cumulative distribution functions (CDF) of ΔId/Id of both the n- and p- MOSFET are shown in Fig.3 (a) and (b), respectively. The drain voltage is 50mV, the gate voltage is from 0.75V to 0.95V and the step is 0.05V at high temperature (125^{o}C). The result shows the ΔId/Id of the p-MOSFET is obviously larger than that of the n-MOSFET. Recently, it is reported that the enhanced Id-RTS by the active trap of MOSFET at the substrate/dielectric interface than that in the dielectric [6~7]. Therefore, the discrepancy is partially due to more traps closer to the Si/SiO2 interface in the p-MOSFET devices compared to the n-MOSFET devices.

It is very important to note that RTS is not only a variability issue, but also a long term of reliability issue, similar to P/NBTI. In P/NBTI test, the stress condition are |Vg − Vt| / oxide electric field = 7 MV/cm and Vd = 0 V at high temperature (125^{o}C). After the long time stress (20k sec), drain current variations are immediately traced RTS with the condition that drain voltage is 50mV, and the gate voltage is 0.95V at high temperature (125^{o}C). Fig. 4 shows the two different mechanisms that can result in random charge effects. One mechanism takes place in fresh devices induced by random process generation traps while the other occurs in stress devices induced by random stress generation traps. They both influence the Id fluctuation in the device. We compare RTS amplitude distributions in fresh devices and in stress devices under both PBTI and NBTI in Fig. 5(a) and 5(b), respectively. In P/NBTI characterization, the generation of random traps cause the ΔId/Id amplitude distribution in both stress devices is enhanced. It is noteworthy that, there is a larger ΔId/Id tail in NBTI stressed devices than PBTI stressed ones. The NBTI stress has a considerably broader amplitude distribution (3σ = 0.519 %) than PBTI stress (3σ = 0.131 %), suggesting that NBTI has a larger impact on CMOS reliability than PBTI due to a larger ΔId/Id. Moreover, we compare the shift of saturation current (ΔId/Id) with drain voltage and the gate voltage is 0.95V between PBTI and NBTI in Fig. 6(a) and (b), respectively. The NBTI one shows more the generation traps than that PBTI one. In addition, NBTI stress in Fig 7(b) has a larger ΔGm than PBTI stress in Fig 7(a). More recently, [8~9] have suggested a electron trapping induce the HK bulk traps for the NMOS, while the PMOS not only generated defects near the IL but also a hole trapping in a critical current path, thus resulting in a larger ΔId/Id of NBTI than that PBTI one.

We estimated the impact of RTS on the lifetime of HK/MG device on the |Vg − Vt| / oxide electric field = 7 MV/cm of PBTI n-MOSFETs and NBTI p-MOSFETs as shown in Fig. 8(a) and Fig. 9(a), respectively. The saturation current (ΔId/Id) with drain voltage and the gate voltage is 0.95V. In general, the lifetime can be extrapolated at drain current degradation at 10 (%). We assumed that ΔId/Id of the n-MOSFET is 0.085 % and 0.131 % at three standard deviations (3σ) in fresh and stress, respectively. Similarly, we assumed that ΔId/Id of the p-MOSFET is 0.243 % and 0.519 % at three standard deviations (3σ) in fresh and stress, respectively. In PBTI characterization, the lifetime by ΔId/Id of the n-MOSFET on the operation due to RTS in fresh base on w/o RTS is –4.79 (%), while on the operation due to RTS in stress base on w/o RTS is –11.58 (%) in Fig. 8(b). In NBTI characterization, the lifetime by ΔId/Id of the p-MOSFET on the operation due to RTS in fresh base on w/o RTS is –17 (%), while on the operation due to RTS in stress base on w/o RTS is –45 (%) in Fig. 9(b). The impact of ΔId/Id due to RTS of the p-MOSFET was found bigger than that of the n-MOSFET. The summary of lifetime and RTS (3σ) of PBTI n-MOSFETs and NBTI p-MOSFETs is in Table I.

4. Conclusion

This work has presented an investigation and a discussion of the impact of positive and negative bias temperature instability (P/NBTI) on the current degradation of the Random Telegraph Signal (RTS) in advanced gate stacks. Our studies use CDF to analyze RTS with considering random process induce traps and random stress induce traps, suggesting that RTS degradation in NBTI devices exhibits a wider amplitude distribution than the PBTI one. Moreover, we estimated the lifetime numerically based on current degradation with or without RTS. Therefore, RTS of the NBTI p-MOSFET has a larger impact on HK/MG dielectric CMOS reliability than PBTI n-MOSFET due to a larger ΔId/Id.

References

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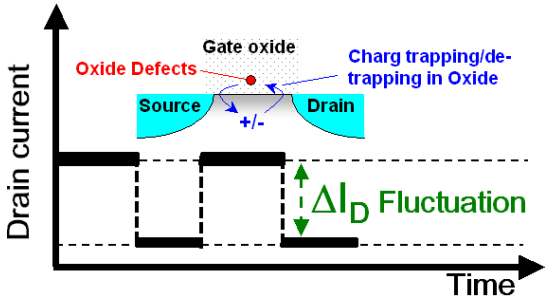

Fig. 1. Id fluctuation is due to RTS.

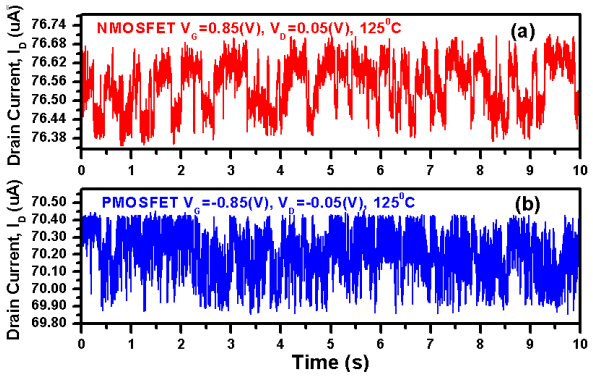

Fig. 2. (a) RTS in nMOSFET devices. (b) RTS in pMOSFET devices.

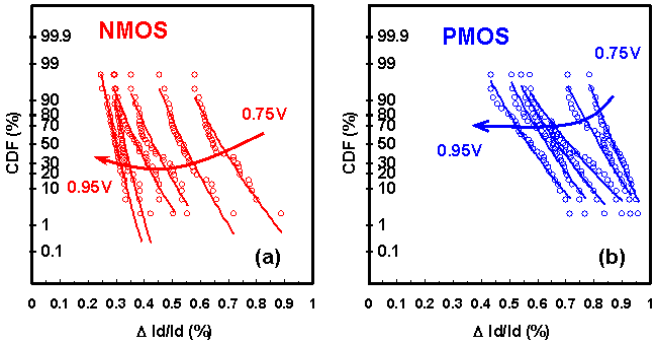

Fig. 3. (a) CDF of charge induced ΔId/Id for RTS in nMOSFET devices. (b) CDF of charge induced ΔId/Id for RTS in pMOSFET devices.

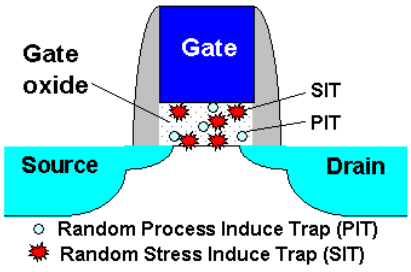

Fig. 4 Random trap generation of the two different mechanisms.

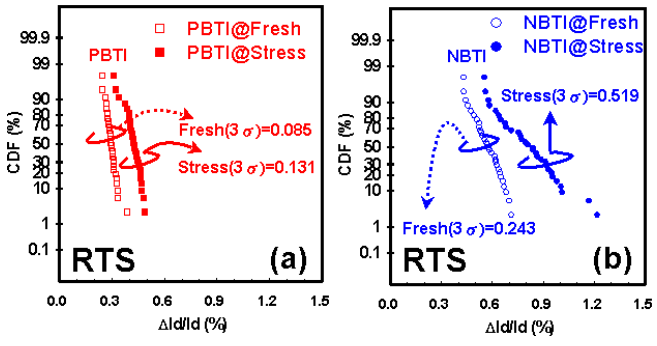

Fig. 5 CDF of charge induced ΔId/Id in fresh devices and stress devices for (a) n-MOSFET and (b) p-MOSFET.

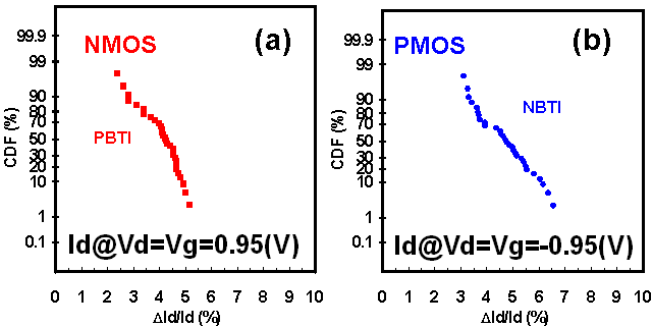

Fig. 6 CDF of charge induced ΔId/Id with drain voltage and the gate voltage is 0.95V for (a) PBTI and (b) NBTI.

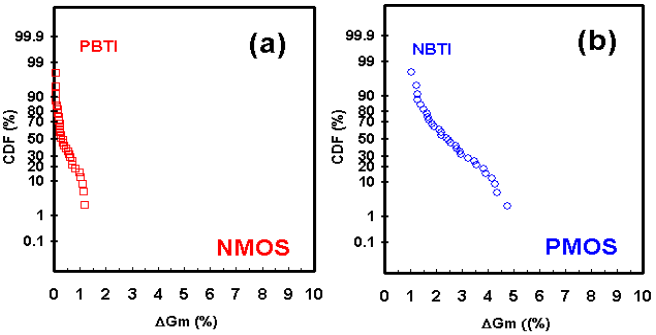

Fig. 7 CDF of charge induced ΔGm for (a) PBTI and (b) NBTI.

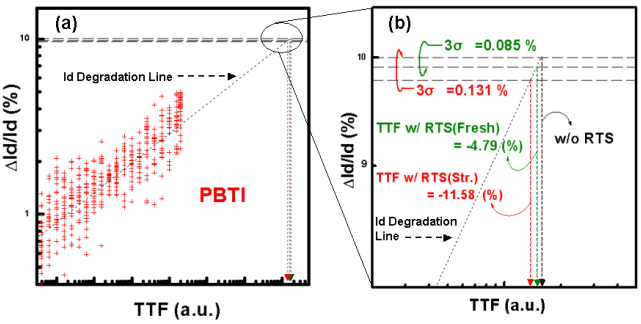

Fig. 8 (a) The PBTI lifetime is numerically based on current degradation of NMOSFET under |Vg − Vt| / oxide electric field = 7 MV/cm. (b) PBTI lifetime with and without RTS.

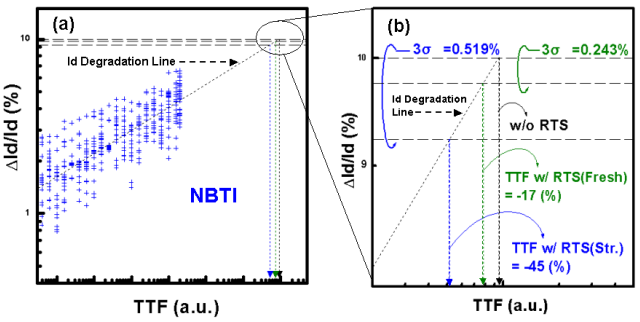

Fig. 9 (a) The NBTI lifetime is numerically based on current degradation of PMOSFET under |Vg − Vt| / oxide electric field = 7 MV/cm. (b) NBTI lifetime with and without RTS.

Device	Lifetime (Base on w/o RTS) (%)		RTS (3σ)	
	w/ RTS(Fresh)	w/ RTS(Stress)	Fresh	Stress
NMOS	-4.79	-11.58	0.085	0.131
PMOS	-17	-45	0.243	0.519

Table I Lifetime and RTS (3σ) of PBTI n-MOSFETs and NBTI p-MOSFETs