Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp128-129

The Experimental Observation of the Process Induced Random Dopant Effect in Trigate MOSFETs

E. R. Hsieh[1], H. M. Tsai[1], Steve S. Chung[1], C. H. Tsai[2], R. M. Huang[2], C. T. Tsai[2], and C. W. Liang[2]
[1]*Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Taiwan* [2]*UMC, Hsinchu, Taiwan*

Abstract- This paper reports a methodology to investigate the dopant fluctuation of trigate devices via a purely experimental approach. The process induced dopant distribution along the channel direction can be determined. Three results were demonstrated: (1) Boron clustering effect in nMOSFETs can be reasonably explained which results in a larger Vth variation, in comparison to that of pMOSFETs; (2) Experiments have been extended to the advanced bulk-trigate CMOS devices and the sidewall roughness effect on trigate has also been evaluated; and (3) The use of the trigate structure in SRAM cell shows good V_{dd} scalability.

1. Introduction

The random dopant fluctuation (RDF), Fig. 1, is one of the most important issues for sub-50nm CMOS technologies in terms of the device architecture and manufacturing with the drastic scaling of CMOS technology. In the past, variations associated with implant and RTA anneal [1-2], the strain effect [3], and gate material [4-5], have been raised up. To solve RDF, carbon co-implant [6], FDSOI or FinFET [7-8], and high-k gate dielectric [9] have been proposed to reduce the variability effectively. However, the understanding of dopant effect on the RDF has been almost studied by the simulations. Not until 2011, the understanding of the RDF became possible by using an experimental approach that we developed in [10].

In this paper, the discrete dopant profiling (**DDP**) technique has been further elaborated on trigate MOSFETs to study the process induced effects such as boron clustering, sidewall roughness effect, and fin-height induced variations. Examination of the SRAM by using the trigate has also been used as a test vehicle to examine the cell performance.

2. Device Preparation

Advanced poly-Si gate bulk planar and trigate CMOS devices, with SiON insulator, were fabricated. Fig. 2 shows the 3D structure and TEM of the bulk-trigate device. The fin width 30nm or 75nm and with various fin heights, 10nm, 15nm, and 30nm, and gate length= 36nm, were chosen. Both control and split are made on the same wafer. An SRAM cell has also been provided as a test vehicle. Devices with different areas were used to calculate the V_{th} variations.

3. Results and Discussion

A. The Method of Dopant Profiling

The principle of **DDP** method is to locate the channel barrier-peak position by varying the source-to-drain bias as shown in Fig. 3 [11]. Fig. 4 shows the drawings of the channel barrier and how to calculate the peak value through the calculation of a varying barrier height from DIBL and lateral length, L_{eff}' such that the peak position can be located. The discrete dopant can be modeled as a delta function derived in Table 1. The local σVth(x) was first calculated and then the concentrations of discrete dopants can be determined. Eq. (5).

B. The Observation of Boron Clustering

The random fluctuation can be gauged by the Pelgrom plot [12] or Takeuchi plot[13]. The first comparison is Pelgrom plot, Fig. 5, in which the V_{th} variation is compared for the control n- and p-MOSFETs. The A_{VT} of nMOSFET is larger than that of pMOSFET. To explain the larger value of nMOS, a boron clustering model was reported in [12]. In general, the boron atoms with high concentration are clustered in Si. Some boron atoms of channel dopants are grouped together with weak bonding and act as one boron cluster which then leads to the larger fluctuation of dopants in the channel.

To prove the existence of the boron clustering, experimental result was demonstrated in Fig. 6, where the large fluctuation in nMOSFETs is observed. Also, very high dopant distributions are found near the drain side that are attributed to the diffused atoms of drain impurities into the channel.

C. The Process Induced Random Dopant in Trigate MOSFETs

The extension of the approach to study the dopant fluctuation in Trigate and the comparison with conventional MOSFET are demonstrated. Fig. 7 shows the comparison of the dopant distribution in conventional and trigate nMOSFETs. It was found that the experimental results of trigate device shows much less fluctuation, which should be from the suppression of the dopant fluctuation by the larger electrical field as a result of a better chancel controllability in the trigate. To study the sidewall roughness effect in trigate (or FinFET) devices, the trigate devices with 3 different fin heights are evaluated. Fig. 8 shows the structure and the profiling results for both n- and p-trigate. It reveals that larger fin height device shows a much larger dopant fluctuation, as a result of the sidewall roughness effect.

D. The SRAM Using Trigate MOSFETs

Fig. 9 shows butterfly curves of the trigate with the SEM shown in Fig. 10. As a benchmark test, with SRAM circuit and WRM defined in Fig. 11, the n-channel cell shows smaller B_{VT} than conventional devices (Fig. 12). Also, the write margin(WRM) has been largely improved as we increase the fin-height or the recessed depth of STI (Fig. 13) since higher fin device provides a better control of the channel.

In summary, an experimental dopant profiling technique has been demonstrated on the advanced trigate devices with focus on the process induced dopant variations. By applying this approach, we may understand: (1) the dopant fluctuation in the channel completely, (2) the boron clustering effect in n-channel devices which explains why the A_{VT} is much larger in n-channel devices, and (3) the sidewall roughness effect in a trigate device. Moreover, the design of SRAM using the trigate is a near future target for the mass production beyond 20nm CMOS technology node. This prelim study provides a valuable information for further implementation of trigate SRAM.

Acknowledgments *This work was supported in part by the National Science Council under contract NSC99-2221-E009-192 and NSC100-2221-E009-016MY3.*

References: [1] T. Tanaka et al., ***IEDM***, 45(1998). [2] I Ahsan et al., ***VLSI***, 170(2006). [3] Y. L. Tsang et al., ***T-ED***, 3040(2007). [4] A. R. Brown et al., ***T-ED***, 3056(2007). [5] Y. Zhang et al., ***IEDM***, 57(2009). [3] T. Tsunomura et al., ***VLSI***, 110(2009). [6] K. J.Kuhn, ***IEDM***, 71(2007). [7] O. Weber et al., ***IEDM,*** 245(2008). [8] S. Kamiyama, ***IEDM***, 431 (2009). [9] E. S. Andres et al, ***IEEE EDL*** p.772(2006). [10] E. R. Hsieh et al., ***VLSI***, 152(2011). [11] E. R. Hsieh et al., ***VLSI***, 189(2012). [12] M J M Pelgrom et al., ***IEEE JSSC***, 1433(1989). [13] K. Takeuchi et al., ***IEDM***, 467(2007).

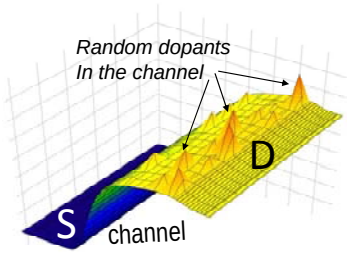


Fig. 1 The schematic of RDF(Randon Dopant Fluctuation, in which the dopants are randomly distributed along the channel.

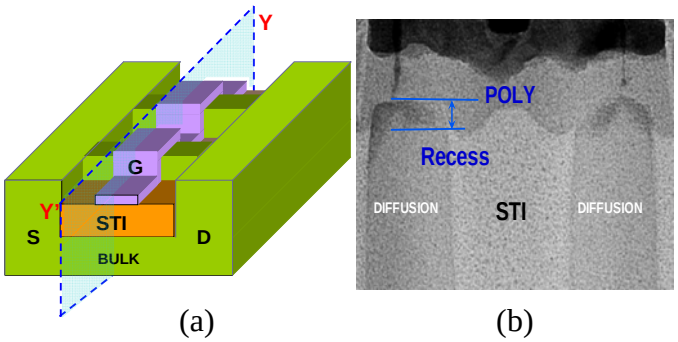


Fig. 2 The trigate structure used in this study. (a) the 3D structure, (b) the TEM cross-section along the Y-Y' direction.

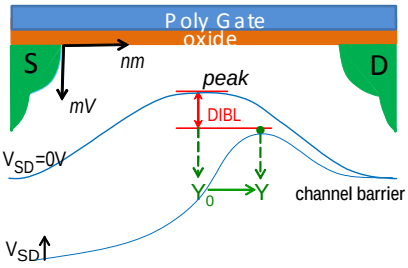


Fig. 3 By varying the V_{SD}, the barrier peak can be found from the DIBL since as V_{SD} increases, the barrier peak will be shifted toward the drain such that the delta trap density can be profiled along the channel.

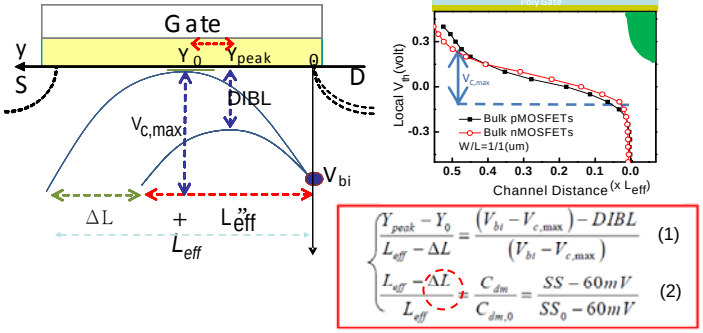


Fig. 4 A new model is to approximate the channel barrier peak as a second degree curve, in which the peak position can be determined from the measured DIBL.

$$\sigma V_{th}(x) = \frac{q}{C_{ox}}\sqrt{\frac{\int_0^{W_{dep}} N_i(x)dx}{LW}} \quad (1)$$

$$= \frac{q}{C_{ox}}\sqrt{\frac{\int_0^{W_{dep}} \Delta n_i(x)\delta(x-x_i)dx}{LW}} \quad (2)$$

$$= \frac{q}{C_{ox}}\sqrt{\frac{\sum \Delta n_i(x_i)}{LW}} \quad (3)$$

$$= \frac{q}{C_{ox}}\sqrt{N_i}(\#/cm^3) \quad (4)$$

$$\rightarrow \quad N_i(x) = \left(\frac{C_{ox}}{q}\sigma V_{th}(x)\right)^2 \quad (5)$$

Table 1 The derivation of dopant denstiy as a function of the V_{th} variation along the channel direction.

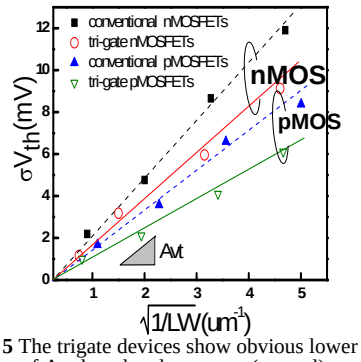


Fig. 5 The trigate devices show obvious lower slopes of A_{vt} than the planar ones (control) because a stronger gate field in trigate tends to inhibit the dopant fluctuation.

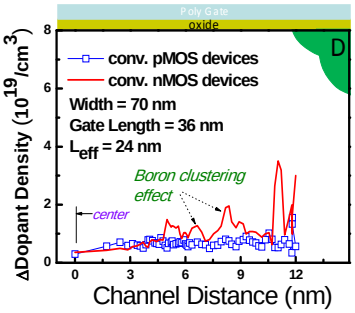


Fig. 6 The experimental delta dopant density of conventional nMOS and pMOS devices. Note that nMOS exhibits a much larger dopant density as a result of the clustering effect.

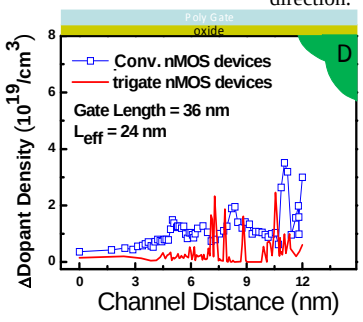


Fig. 7 The experimental delta dopant density of conventional and trigate nMOS devices. Note that trigate device exhibits a smaller delta dopant density as a result of a larger electrical field effect.

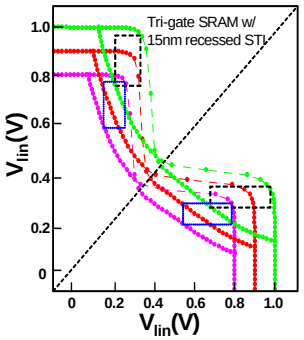


Fig. 9 Butterfly curves of a recessed tri-gate with good SNM for V_{DD} scaling.

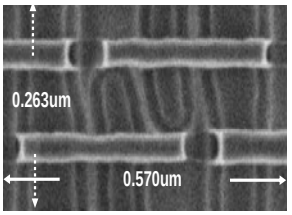
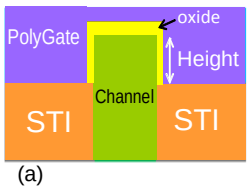
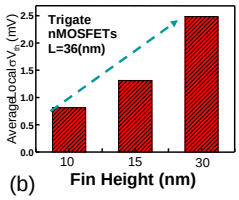
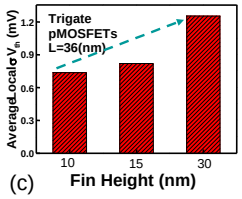
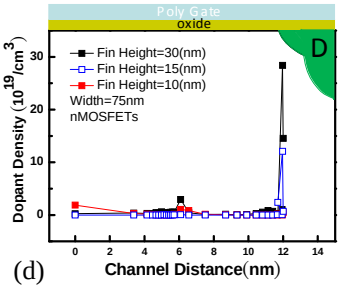


Fig. 10 SEM top-view of SRAM cell. The size of the cell is 0.149um^2.









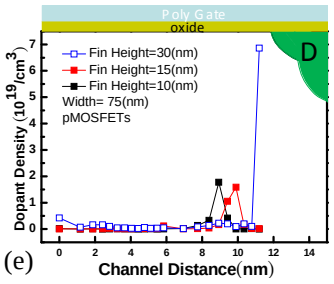


Fig. 8 (a) The trigate with various heights. Local Vth variations in (b) nMOSFET, (c) pMOSFETs, and the dopant density of trigate devices in (d) nMOSFETs, (e) pMOSFETs. Larger fin height induces larger dopant variation.

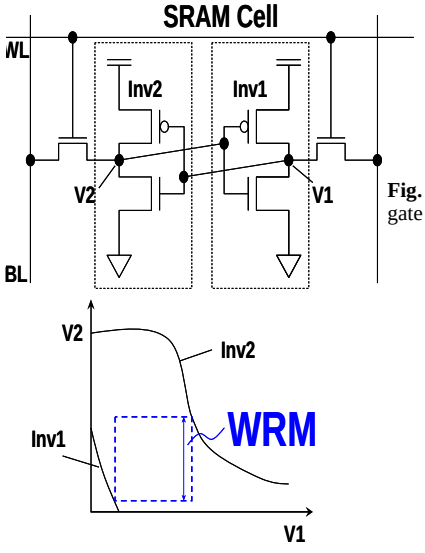


Fig. 11 (top) The schematic of SRAM circuit; (bottom) Definition of WRM (write margin).

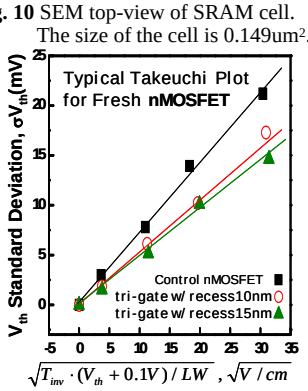


Fig. 12 Comparison of B_{VT} for control and tri-gate nMOSFETs with different Fin-heights.

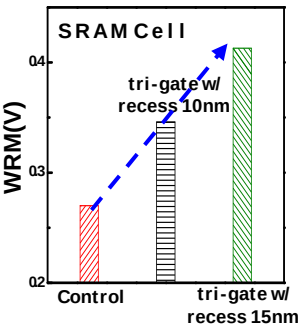


Fig. 13 Comparison of WRM for control SRAM and trigates with different Fin heights (recessed).