Epitaxial Tunnel Layer Structure for Complementary Tunnel FETs Enhancement

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1. Introduction

As the CMOSFET scales down rapidly, the power consumption becomes a critical issue for low power ICs [1]. The non-scalable subthreshold swing (S.S.) of conventional MOSTETs makes the difficulty of the voltage scaling. Tunnel FET (TFET) has the advantages of low leakage current and low S.S. behavior but suffers from low oncurrent and poor average S.S. [2-6]. Different architectures to improve TFET performance have been proposed [7-8]. Using low band-gap materials as the TFET source is also a popular way to enhance the TFET on-current [9]. However, the hetero-structure source needs two different materials for N-TFET and P-TFET, for example Ge for N-TFET and In_xGa_{1-x}As for P-TFET. [10]. In this work, we propose a novel structure with epitaxial-tunnel-layer (ETL) using only one low band-gap material to enhance both P-TFET and N-TFET performance.

2. Device Structure

Sentaurus-TCAD tool was used in this work [11]. Fig.1. shows the schematic structure of the ETL-TFET and the normal TFET. The material of the ETL is intrinsic silicon or Si_{0.7}Ge_{0.3}. The channel length is 60 nm with a doping concentration of 1×10^{15} cm⁻³. The SiO₂ gate dielectric is 2-nm-thick. The source/drain doping concentration is $1x10^{20}/1x10^{18}$ cm⁻³ for N-TFET and $1x10^{18}/1x10^{20}$ cm⁻³ for P-TFET. The lower doping concentration is used to suppress the ambipolar characteristic. The gate work-function is 4.05eV for N-TFET and 5.15eV for P-TFET. The dynamic nonlocal tunneling model with default indirect BTBT parameters in TCAD is applied. The important device and simulation parameters are listed in Table 1. Complete recombination model, mobility model and Fermi distribution are all considered. The gate tunneling leakage current is ignored in this work.

3. Results and Discussions

Fig.2 shows the transfer characteristics of the normal TFET and the ETL-TFET. The ETL structure exhibits better on-current performance because the tunneling orientation of ETL-TFET is the same as the electric field direction modulated by gate which makes the gate modulate the potential more effectively. In addition, because the tunneling is designed to occur in the ETL region, introducing the SiGe material could enhance both N-TFET and P-TFET performance due to band-to-band-tunneling (BTBT) in the SiGe layer. Although the lower band-gap of SiGe induces higher generation current, the

ETL-SiGe-TFET has low off-current due to the small area of the SiGe ETL comparing to the whole channel.

Fig.3 compares the ambipolar current characteristics of the normal TFET and the ETL-Si-TFET. The ETL structure with low doping design could eliminate the ambipolar characteristic much obviously than the normal TFET because of the strong reduction of the electric field in the ETL. Fig.4 shows the ambipolar BTBT profiles for the normal TFET and the ETL-Si-TFET. It indicates that the ETL-Si-TFET has no vertical BTBT in ETL and much smaller parallel BTBT in channel region than the normal TFET. The vertical BTBT is suppressed by the lower source/drain doping concentration which reduces the electric field in the ETL significantly and the parallel BTBT in channel is suppressed because the ETL shields the channel potential modulation by gate.

Fig.5 and Fig.6 show the effect of the ETL thickness. It is observed that improper ETL thickness design would degrade the on-current due to the increase of electric field in thick ETL. The NTFET with SiGe ETL structure exhibits a current kink in the transfer characteristic. This is explained by the schematic diagram in Fig.7. At first, the BTBT occurs from the valance band of the Si channel to the conduction band of the SiGe ETL, and then, with more band bending modulated by the gate, the BTBT in the SiGe layer occurs and thus enhances the on-current strongly which induces the current kink characteristic. The kink characteristic is not observed on the device with 2-nm-thick SiGe ETL because the SiGe ETL thickness is too thin to occur BTBT.

Fig.8 shows the on-current and the average S.S $(10^{-15} \sim 10^{-9} \text{ A/}\mu\text{m})$ of the ETL-SiGe-TFET. It is observed that the optimized ETL thickness is 4 nm for on-current and 6 nm for average S.S. The significant average S.S. improvement for NTFET is due to the earlier occurrence of BTBT which is consistent with kink point in Fig.6. The on-current and average S.S both degrade at too thick ETL due to the electric field degradation.

4. Conclusions

In this work, TFET architecture named ETL-TFET is proposed. The ETL structure could enhance the on-current and eliminate the ambipolar characteristics. By introducing a SiGe ETL, both the N-TFET and P-TFET performance could be improved. The tradeoff between the on-current and the average subthreshold swing is presented and explained. For low power application, the ETL structure with low band-gap material integration is very promising

for TFET performance enhancement. Acknowledgement

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References

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Table 1 Device structure and dynamic

Dynamic nonlocal BTBT parameter

nonlocal BTBT parameters.

Channel Thickness

Source/Drain Overlap

Spacer Length

ETL TFET

Intrinsic Si/SiGe ETL

(right).

Apath

 $\frac{\text{Bpath}}{\Delta \text{C}}$

ε_{op}

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20 nm

10 nm

5 nm

4.0x10¹⁴ cm⁻³s

 $1.9 \text{ x} 10^7 \text{ cm}^{-3} \text{s}^{-1}$

Normal TFET

Gate

 $0 \,\mathrm{eV}$

0.037 eV

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Fig.1 Schematic structure of the ETL-

TFET (left) and the Normal-Si-TFET

Fig.2 Transfer characteristics of ETL-TFET and the Normal-TFET.



Fig.3 Ambipolar characteristics of the P-TFET (upper) and the N-TFET (bottom).



Fig.5 Transfer characteristics of the ETL TFET with different Si ETL thicknesses.



Fig.6 Transfer characteristics of the ETL TFET with different SiGe ETL thickness. Current kink is observed on N-TFET.



Fig.7 Schematic band diagram explaining the kink characteristic of the N- TFET SiGe ETL.



Fig.8 On-current and average S.S as a function of the ETL thickness.