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EOT Scaling in Tunnel Field-Effect Transistors: Trade-off between Subthreshold Steepness and Gate Leakage

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1. Introduction

Conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) are rapidly reaching their fundamental physical limits to maintain low-power consumption. The difficulties they face are the degradation of subthreshold swing (SS) and increase in OFF-current (I_{off}). A tunnel field-effect transistor (TFET), which is a quantum mechanical device, is a promising candidate for the basic element of large scale integration (LSI) systems in the coming power-consumption era. The advantage of TFETs is that they have subthreshold characteristics that allow them to access SS with less than 60 mV/decade, which is the fundamental limit of conventional MOSFETs. Several research groups have already reported experimental demonstrations of the sub-60 mV/decade TFET operation [1]. The urgent research issue of TFETs is ON-current, which is still a few orders of magnitude less than that of conventional MOSFETs.

An equivalent-oxide-thickness (EOT) scaling is crucial to boost ON-current and obtain steeper SS because it directly enhances the gate electrostatic control. For SS, one can easily understand the importance of gate governance from the following equation [2]:

$$SS \equiv \frac{\partial V_g}{\partial(\log I_d)} = \frac{\partial V_g}{\partial \psi_S}\frac{\partial \psi_S}{\partial(\log I_d)},$$

where V_g is the gate voltage, ψ_s is the surface potential, and I_d is the drain current. The first term denotes the gate governance to the channel, and the second term expresses the current flow mechanism. EOT scaling can minimize the gate governance term, resulting in steeper SS characteristics.

On the other hand, simple EOT scaling accompanies gate leakage enhancement. Reports on gate leakage problems in TFETs do not currently exist. TFETs could be considered as similar to conventional MOSFETs; however, their gate leakage currents could differ from each other.

In this presentation, we discuss EOT scaling in TFETs, as well as its advantages and disadvantages, on the basis of the experimental data and simulation. Furthermore, we first examine gate leakage in TFETs and discuss the discrepancy in the gate leakage current between TFETs and conventional MOS devices.

2. Experiment and Simulation

TFETs were fabricated on silicon-on-insulator (SOI) wafers with local-oxidation-of-silicon (LOCOS) isolation. The TFETs were P-type devices that had N^+-sources and P^+-drains and turned on with negative gate bias. The devices had a gate length of 10 μm and a gate width of 10 μm. They had HfO_2-based gate dielectrics with varied EOTs with a minimum of 0.9 nm [3]. The gate metal was TaN. The simulation was performed by using HyENEXSS™ [4] including our original non-local tunneling module that considered the tunneling direction. The device structure was reproduced by process simulation. The impurity profiles were well verified by secondary-ion-mass-spectroscopy (SIMS) measurements.

3. Results and Discussion

The advantages and disadvantages of EOT scaling appear as a trade-off between the SS value and the amount of gate leakage current. Figure 1 shows the simulation summary of SS and the gate leakage current with variation in EOT. EOT scaling drastically reduces SS, and, on the other hand, increases the gate leakage current. The EOT scaling is quite effective to clear the necessary condition of TFETs, which is an SS less than 60 mV/decade. We note that EOT scaling is not the only way to achieve the sub-60 mV/decade operation. For example, we can clearly see that the pn junction steepness could be important for the subthreshold characteristics. An elaboration of the pn junction could complement EOT scaling and increase the required oxide thickness to achieve the sub-60 mV/decade operation.

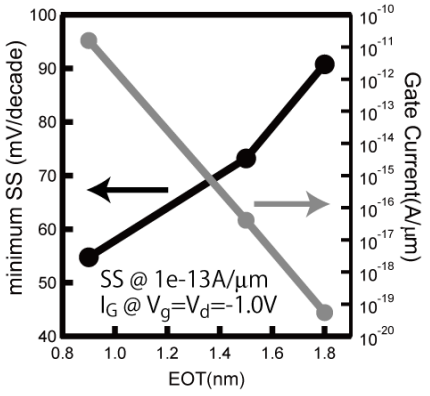

Fig. 1 Simulation summary of the minimum SS and the gate leakage with varying EOT. The simulated device structure was based on the fabricated structure.

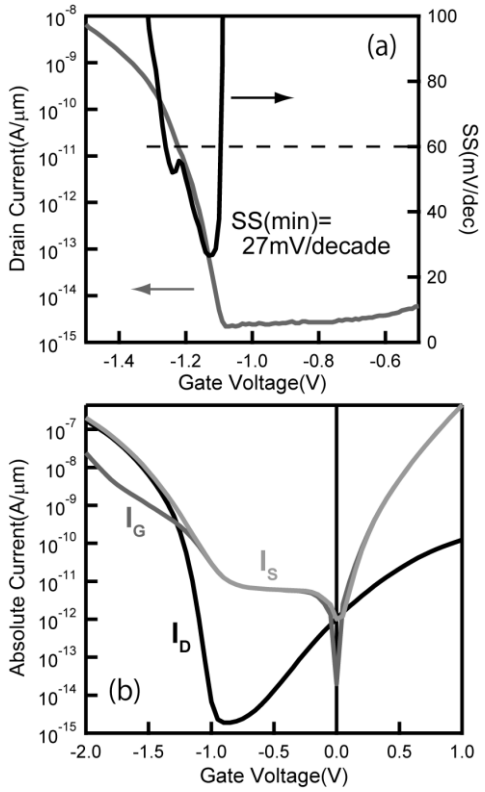

Fig. 2 Experimental I-V_g curves with V_d = -1.0 V. (a) I_d-V_g curve around the turn-on voltage. (b) I_d, I_s, I_g-V_g curves.

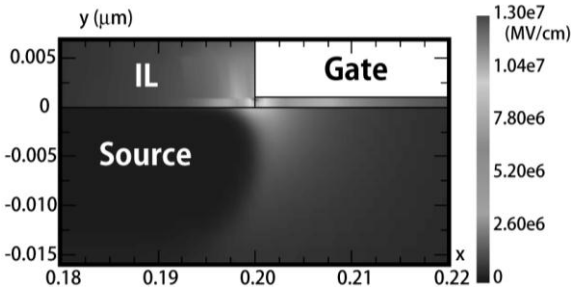

Fig. 3 The strength distribution of the electric field near the source-side edge of the gate, with V_d = V_g = -1.0 V. A strong electric field was observed at the edge.

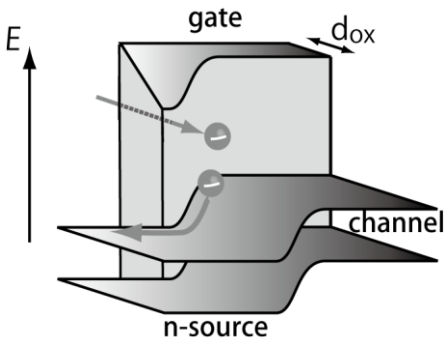

Fig. 4 A schematic of the band line-up among the source, channel, and gate. The gate-leakage path is indicated by arrows: electrons tunnel through the source-side of the gate dielectric and then flow into the source.

The experimental demonstration of the sub-60 mV/decade operation with EOT scaling is shown in Figure 2. The EOT was scaled down to 0.9 nm. The minimum SS was 27 mV/decade as shown in Figure 2(a). The sub-60 mV/decade performance was highly reproducible; however, the variability exceeded that of conventional MOSFETs fabricated on the same wafer. The origin of the variability of TFETs is currently being investigated, and it will be reported later.

EOT scaling aided in the steep turn-on of the drain current, whereas the source current was degraded by the gate leakage current (Figure 2(b)). The leakage current flowed from the gate to the source in the V_g range near turn-on, which was confirmed by its insensitivity to the drain voltage. With regard to our devices, an increase in the metal work function is needed to optimize the turn-on voltage, which might reduce the gate leakage current. In general, development of a higher-k gate oxide technology might be awaited from the viewpoints of both the ON characteristics and the gate leakage problem.

The leakage situation of TFETs was investigated by simulation, and it was found to be different from that of conventional MOSFETs. Figure 3 shows the strength distribution of the electric field near the source-side edge of the gate. A strong field can be observed at the edge, which results in strong gate leakage dominated by the edge leakage component. The case is quite different from that of MOSFETs, which are dominated by areal leakage. Considering both the experimental and the simulation results, we believe that the dominant leak carrier is an electron, which flows as shown in Figure 4.

4. Conclusions

We have investigated the EOT scaling issue in TFETs using both an experiment and a simulation. EOT scaling aids in achieving a steep SS, which was experimentally demonstrated with the 27-mV/decade operation of a P-TFET. EOT scaling accompanies gate leakage. The leakage situation was first revealed by simulation. Dominant leakage occurs on the source-side edge of the gate. This case is quite different from that of conventional MOSFETs.

Acknowledgements

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References

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