Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp76-77

Compound Semiconductor Tunneling Field-Effect Transistor Based on Ge/GaAs Heterojunction with Tunneling-Boost Layer for High-Performance Operation

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1. Introduction

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are facing scaling-limit due to critical reliability and process issues such as short channel effects (SCEs), shallow junction formation, and optical limit in photolithography. To overcome the scaling limits, various devices based on novel structures, materials, and mechanisms have been researched. The tunneling field-effect transistor (TFET) is one of the solutions due to its excellent subthreshold swing (SS) and low off-state current (I_{off}) [1]. In spite of these advantages, low on-state current (I_{on}) and operation speed have been pointed as drawbacks that silicon (Si) TFET is bearing. I_{on} can be significantly improved by introducing a new channel material, doping profiling, and varying gate dielectric, combinationally [2-5]. If the channel is made from direct-bandgap compound semiconductor, electron mobility can be greatly enhanced and integration with optical and photonic systems (light sources are mostly from those materials) will be more expectable.

In this work, we have proposed and characterized a Ge/GaAs heterojunction TFET having a tunneling-boost layer (Ge/n-GaAs/p-GaAs/GaAs). 3-dimensional (3D) device simulations were performed for the device design in terms of I_{on}, threshold voltage (V_{th}), and high-frequency current gain (f_T) [6]. It was shown that controls over lengths of the boosting layer (thin n^+ GaAs layer) and lightly doped p-type channel (p^- GaAs) had effects in adjusting V_{th} and current drivability without complications for shifting metal workfunction.

2. Device Design and Performances

We characterized TFETs in the proposed structure by device simulations (TCAD and ATLAS) activating multiple models in use for higher accuracy. Fig. 1 illustrates a schematic of vertical nanowire TFET with functional doping. Ge and GaAs are almost lattice-matched materials that can be epitaxial growth with acceptable interfaces and doping types and profiles are determined by *in situ* doping. Doping concentrations of p^+ Ge (source), n^+ GaAs (source-side channel), p^- GaAs (drain-side channel), and n^+ GaAs (drain) are 1×10^{20} cm^{-3}, 1×10^{19} cm^{-3}, 1×10^{16} cm^{-3}, and 1×10^{18} cm^{-3}, respectively, in sequence. The channel length, radius, and gate oxide thickness are 50 nm, 10 nm, and 2 nm, respectively. The workfunction of gate metal (Φ_m) is 4.34 eV.

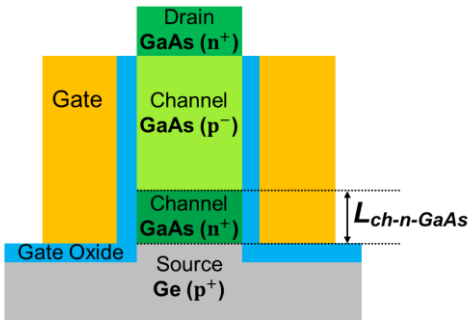
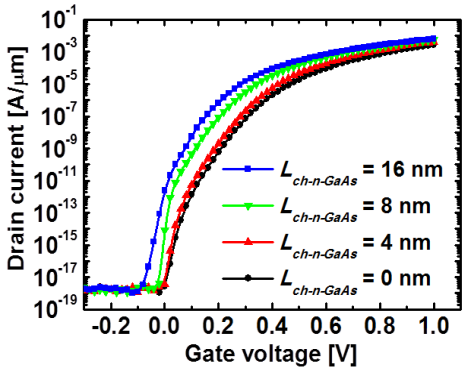
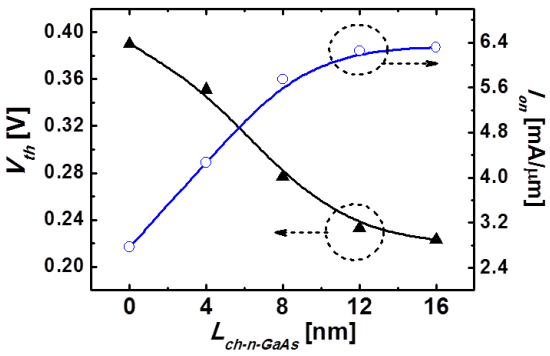


Fig. 1 Structure of Ge/n-GaAs/p-GaAs/GaAs TFET.



(a)



(b)

Fig. 2 Direct-current characteristics. (a) I_D-V_{GS} transfer curves at different $L_{ch\text{-}n\text{-}GaAs}$'s. (b) V_{th} and I_{on} as a function of $L_{ch\text{-}n\text{-}GaAs}$.

Fig. 2(a) shows the drain current (I_D) vs. gate-to-source voltage (V_{GS}) transfer curves. As the length of n^+ GaAs channel (top of p^+ Ge source in Fig. 1), $L_{ch\text{-}n\text{-}GaAs}$, increased, I_{on} monotonically increased. Fig. 2(b) plots V_{th} and I_{on} for

various $L_{ch\text{-}n\text{-}GaAs}$ values. As $L_{ch\text{-}n\text{-}GaAs}$ increased, I_{on} also increased in accordance, up to 6.3 mA/μm while V_{th} decreased monotonically down to 0.24 V. I_{on} and V_{th} are defined as the drain current at $V_{GS} = V_{DS} = 1$ V and V_{GS} at $I_D = 10^{-7}$ A/μm (by the constant current method), respectively. It is observed that the length modulations of n/p-GaAs channel regions adjust V_{th} without changing Φ_m.

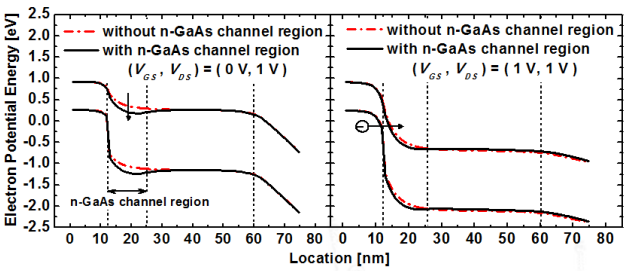


Fig. 3 Energy-band diagram at the off- and on-states.

Fig. 3 demonstrates the simulated energy-band diagrams of the proposed TFET at the off- (left) and on-states (right). In cases of both the states, tunneling barrier width between source and channel regions becomes thinner by introducing n-GaAs region. However, I_{off} and ambipolar behavior in the negative V_{GS} region (off-state and below) are effectively suppressed regardless of $L_{ch\text{-}n\text{-}GaAs}$ since the band-to-band tunneling probability at drain side is substantially low due to the large energy bandgap of GaAs (E_G = 1.42 eV). On the other hand, the tunneling barrier is very narrow at an on-state and its further thinning by n-GaAs layer, which boosts the tunneling rate and I_{on}, consequently.

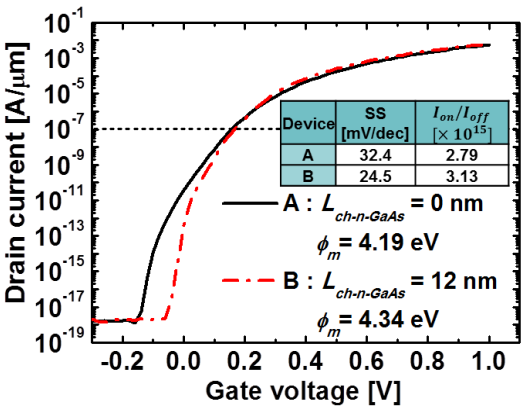


Fig. 4 I_D-V_{GS} curves for devices with a V_{th} and different $L_{ch\text{-}n\text{-}GaAs}$'s.

Fig. 4 shows I_D-V_{GS} curves for devices with the same V_{th}'s and different $L_{ch\text{-}n\text{-}GaAs}$'s. Φ_m's were controlled to adjust V_{th}'s to be the same. The values of average subthreshold swing (SS) and on/off current ratios (I_{on}/I_{off}) for each device are summarized in the table in Fig. 4. SS was extracted as the average slope between two points of onset V_{GS} and V_{GS} at a reference current, $I_D = 10^{-7}$ A/ μm. The average SS above the onset V_{GS} shows the improved subthreshold characteristics of the TFET with n-GaAs channel region.

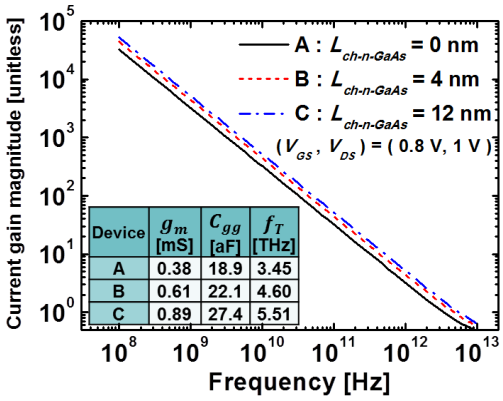


Fig. 5 f_T as a function of frequency with different $L_{ch\text{-}n\text{-}GaAs}$'s.

Fig. 5 shows the high-frequency current gain (f_T) as a function of small-signal frequency. As shown in the figure, f_T was improved as $L_{ch\text{-}n\text{-}GaAs}$ increased as a result of enhancement of transconductance (g_m) and the linearly proportional relation between g_m/C_{gg} and f_T [7]. The C_{gg} means the total value of intrinsic gate-to-drain capacitance (C_{gd}) and gate-to-source capacitance (C_{gs}). It turns out that the n-GaAs channel region has more significant influence on g_m than the C_{gg}. Current gain plot in Fig. 5 supports that the proposed TFET has superiority in radio-frequency (RF) performances as well as DC characteristics. It is observed that f_T of the proposed TFET with $L_{ch\text{-}n\text{-}GaAs}$ = 12 nm is 5.51 THz at V_{GS} = 0.8 V and V_{DS} = 1.0 V.

3. Conclusions

A tunneling field-effect transistor based on functionally doped Ge/GaAs heterojunction has been proposed and evaluated by 3D device simulations. It was verified that the V_{th} was adjustable by controlling the n^+ GaAs channel length. Introducing this region improved DC device performances such as current drivability and output swing and RF performances as well. With an n-GaAs length of 12 nm, I_{on} of 6.3 mA/μm and f_T of 5.51 THz were obtained.

Acknowledgements

This research was supported by the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (MEST) under Grants 2011-0025701 and 2011-0016222. Dr. Cho is supported by NRF Grant funded by the Korean Government (NRF-2011-357-D00155).

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