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Low Leakage Junctionless Vertical Pillar Transistor

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1. Introduction

For sub-30nm DRAM technology, vertical pillar transistor (VPT) is regarded as the most promising candidate for cell transistor in the $4F^2$ cell array architecture due to its excellent gate controllability which enhances the subthreshold characteristics [1]. With critical scaling of devices, junctionless transistor can be applied when the body of semiconductor is thinner than 20nm allowing for full depletion condition in the channel region as the device is turned off [2] (Fig 1). In this work, we investigate the GIDL phenomena by simulation and demonstrate an extremely low leakage junctionless VPT with partially recessed drain design.

2. Device simulation

3D schematic view and the cross-section of the simulated device are depicted respectively in Fig 2(a) and (b). The gate length (L_g) and the diameter (D) are 80nm and 15nm. The gate oxide thickness (T_{ox_gate}) is 4nm following the ITRS roadmap. The diameter (*d*) and length ($L_{\_r\text{-}drain}$) of the recessed drain are 8nm and 20nm. The uniform doping concentration of $10^{19}cm^{-3}$ is thorough out the S/D and the channel region. The simulation results are calculated by introducing the drift-diffusion model, the doping concentration dependent, and the normal electric field dependent mobility model. SRH and band to band tunneling (BTBT) recombination/generation are also applied to account leakage currents. Moreover, the quantum effect is also included by introducing the density gradient model in the recessed drain region where the recessed diameter is below 10nm.

Fig 3 shows the I_d-V_g characteristics of the junctionless VPT with and without the recessed drain design and the inversion-mode VPT respectively. Traditionally, the inversion-mode devices suppress the gate induced drain leakage (GIDL) by the drain underlap and the LDD. The GIDL of the device without recessed drain is near 10^{-13}A due to its high channel doping. The device with recessed drain design can significantly improve the GIDL due to its smaller peak electric field in Si preventing BTBT from massively occuring at off-state bias.

Fig 4 and Fig 5 shows the transfer characteristics with recessed drain design which has different oxide thickness ($T_{ox\_r\text{-}drain}$) and different recessed diameter. The device with smaller recessed diameter will have smaller GIDL due to the gate contact is away from the drain contact, but the on-state current will be degraded seriously when the recessed diameter is smaller than 6nm due to quantum effect. Moreover, the device with the thicker recessed oxide thickness ($T_{ox\_r\text{-}drain}$) can suppress leakage considerably with sacrificing a few amount of on-state current.

Fig 6(a) and (b) show the electric field distribution of the conventional device and the recessed drain device. With the conventional junctionless device turned off (V_{gs}=0), the peak electric field resulting from the bias of the gate and the drain is mainly located in the Si body. It will cause severe BTBT. In the same bias condition, the peak electric field in the device with recessed drain design is not located exclusively in the Si body but also the oxide between the drain and the channel region. Fig 7(a) and (b) represent the BTBT generation rate distribution, which is the dominant mechanism of the off-state leakage. BTBT generation decreases in the Si body with smaller electric field (Fig 6(a) and (b)). Therefore, in the device with recessed drain design, the GIDL is drastically improved.

To observe the dynamic retention characteristics, Fig 8 shows the result of the transient simulation. The capacitor on the storage node (SN) is charged up to 1V. When the cell transistor is turned off, holes generated by GIDL accumulate in the channel, BJT current would be triggered by the bit line bias variation, and lowers the potential of SN. Decreasing the leakage current would be an effective solution to reduce the parasitic BJT in floating- body devices [3]. The GIDL of the VPT with recessed drain design is significantly suppressed to the order below 10^{-16}A. As a result, the dynamic retention characteristic is improved by applying the recessed drain design.

3. Conclusion

In this work, we demonstrate a low leakage junctionless VPT by reducing the diameter of the drain near the channel with recessed oxide. The GIDL of the cell transistor is well suppressed. Dynamic retention characteristics is also improved due to the suppressing BJT parasitic current during the variation of bit line bias.

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Reference:

[1] H. Chung et al., "Novel $4F^2$ DRAM Cell with Vertical Pillar Transistor(VPT)," in Solid-State Device Research Conference (ESSDERC), 2011 Proceedings of the European, pp. 211 – 214.

[2] A. Kranti et al., "Junctionless nanowire transistor (JNT): Properties and design guideline," in Proc. ESSDERC Conf., 2010, pp. 357–360.

[3] S. Hong, "Memory technology trend and future challenges," in IEDM Tech. Dig., Dec. 2010, pp. 12.4.1–12.4.4

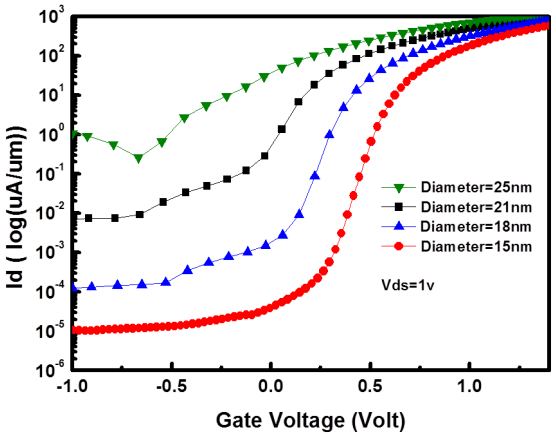

Fig.1 Transfer chracteristics for different diameter of junctionless VPT. The uniform doping concentration of 10^{19} cm^{-3} is used.

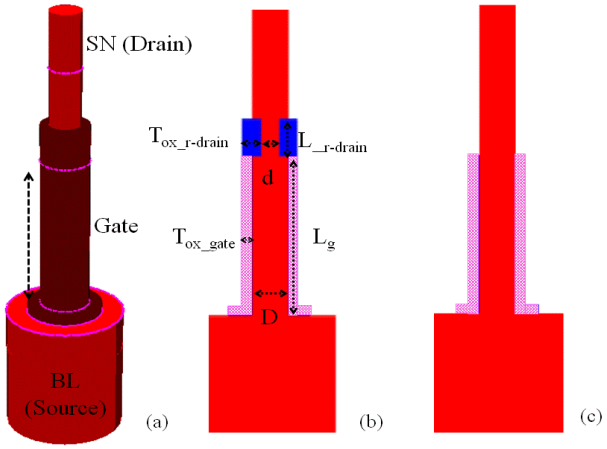

Fig.2 (a) The 3D VPT structure. (b) The cross-section of the device recessed drain design. (c) The cross-section of the device without recessed

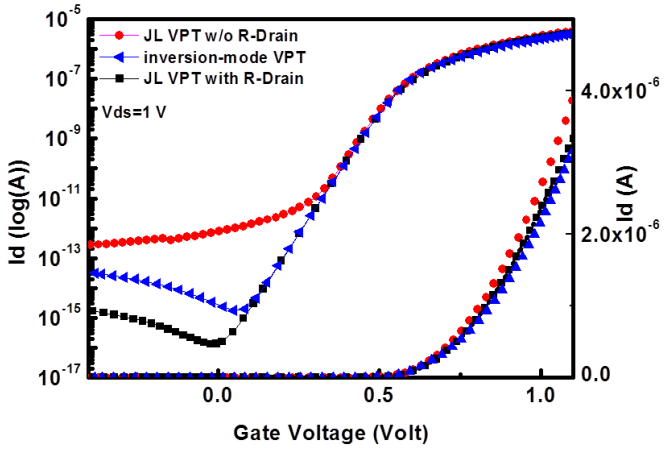

Fig.3 I_d-V_g for the junctionless VPT with and without the recessed drain as well as the inversion-mode VPT.

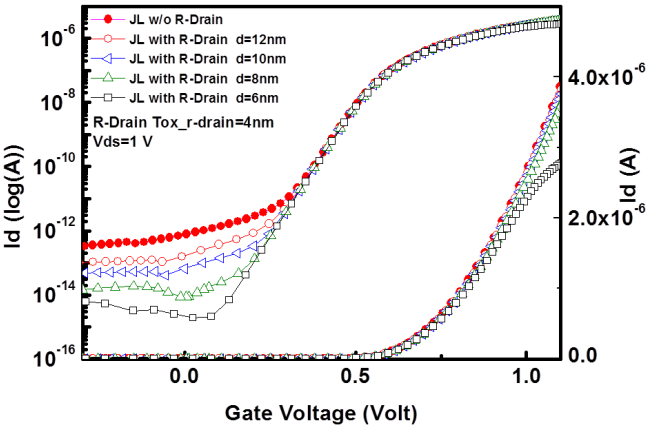

Fig. 4 I_d-V_g for different recessed drain diameter (*d*). The $T_{ox\_r\text{-}drain}$ is 4nm.

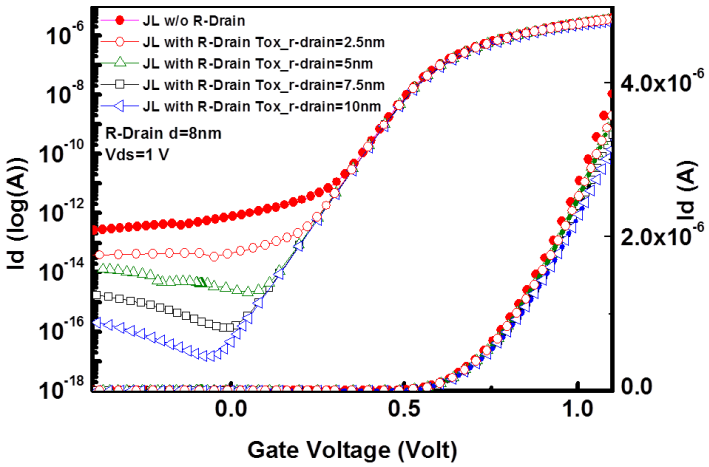

Fig.5 I_d-V_g for different $T_{ox\_r\text{-}drain.}$ .The diameter of the recessed drain is 8nm.

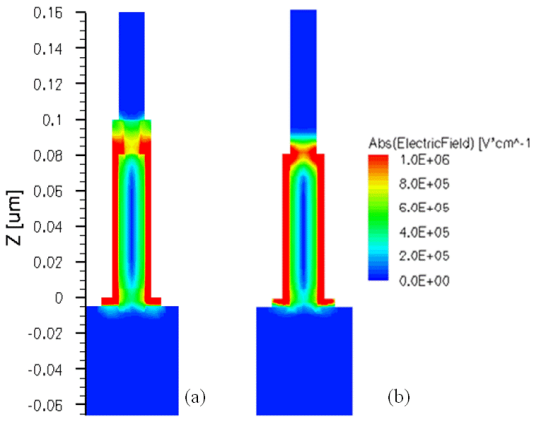

Fig.6 Electric field distribution of (a) a recessed device and (b) a conventional device.

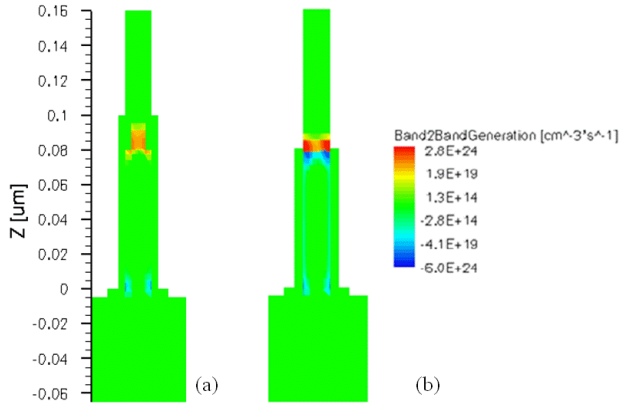

Fig.7 Band to band generation rate distribution

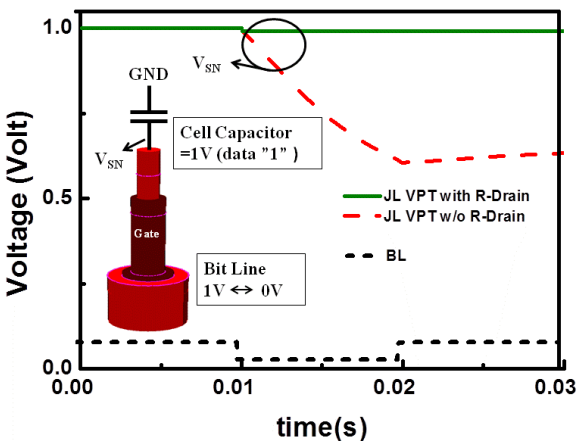

Fig.8 Transient simulation of the transition operation.