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Improved Memory Characteristics of A Novel TATHOS-Structured Charge Trapping Memory

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I. Introduction

With the development of the nonvolatile memory technology, the charge trapping memory (CTM) has attracted much attention due to its higher performance than the conventional gate flash memory device as well as its scalability, immunity from severe reliability and lower program/erase voltages [1-4]. CTM allows a thinner tunneling layer because of the discrete trap charge location in the charge trapping layer which largely avoids the discharge path. The thin tunneling layer could increase the program/erase speed, but it results in degraded retention characteristics simultaneously. To achieve both higher program/erase speed and better retention characteristics, the improved stack structures [5-7] for the tunneling layer have been developed as well as materials choice for the charge trapping layer. Based on our previous simulator [8, 9] which has been calibrated with the experiment data [10], we evaluate the performance of CTM with HfO_2/SiO_2 stack as the tunneling layer and TiO_2 as the charge trapping layer. It is a powerful tool for evaluating the program/erase/retention performance under different gate layers' thicknesses and materials, charge trap densities and distributions, bias voltages and temperatures.

II. Physical Model and Simulation Method

The developed self-consistent simulator has included the crucial physical mechanisms in CTM: trap assisted tunneling (TAT), direct tunneling/F-N tunneling (DT/FN), thermionic emission and relaxation transport which describe the carriers' process across the gate stack layers; recombination, Poole-Frenkel, thermally assisted tunneling and thermal excitation that happen in the charge trapping layer. With this method, we could exact the threshold voltage (Vth), electric potential, electric field and charge trap density's variation with time under different conditions.

In this work, we evaluate the program/erase/retention performance of $TaN/Al_2O_3/TiO_2/HfO_2/SiO_2/Si$ (TATHOS) structure illustrated in Fig. 1(a), which is compared with $TaN/Al_2O_3/TiO_2/SiO_2/Si$ (TATOS) structure in Fig. 1(b). The blocking oxide/charge trapping layer thicknesses are 16/6.5nm for both structures and their gate dielectric layer's equivalent oxide thickness (EOT) are the same except for especial illustrations. The EOT of the stacked tunneling layer is set 4nm. The SiO_2 thicknesses in TATHOS structures labelled by TATHO(2)S and TATHO(1.5)S are 2nm and 1.5nm respectively. The default parameters used in this work are listed in TABLE I.

III. Results and Analysis

The program/erase performance of the TATHO(2)S, TATHO(1.5)S and TATOS structures under various gate voltages is shown in Fig. 2 and Fig. 3, from which we can see that the TATHO(1.5)S corresponds to the highest speed. In the tunneling process across the stacked tunneling layer during program/erase, DT/FN and TAT effects are the main impact factors. Fig. 4(a) and (b) show the shift of gate electric potential for TATHO(2)S and TATOS during the program with 14V gate voltage. It can be analyzed that the TAT effect is decreasing during the program for TATHO(2) and TATHO(1.5) due to the up shift of the electric potential, but the DT/FN only need to tunnel through a very thin layer because of the big barrier between the HfO_2/SiO_2 layer and positive gate voltage. This is the source of two types of speed slope during program/erase for TATHOS. In TATOS the tunnelling layer need to tunnel through is thicker as shown in Fig. 4(b) which could weaken the DT/FN probability badly. To make this phenomenon clearer, we compare the program/erase performance with and without the TAT mechanism as shown in Fig. 5. The same explanations are applicable to the erase process as shown in Fig. 3. The retention characteristics of the high Vth state and low Vth state under different temperatures for TATHO(2)S, TATHO(1.5)S and TATOS structures while time up to 10^8s is shown in Fig. 6, from which we can see that significantly improved retention characteristics are achieved in the TATHO(2)S and TATHO(1.5)S compared to the TATOS. Fig. 7 illustrates the electric potential of TATHO(2)S with 0V gate voltage and we can see that the thick HfO_2 layer effectively reduces the discharge probability due to the barrier between the TiO_2 and HfO_2 layers. Additionally, the program/erase performance of TATOS and $TaN/Al_2O_3/Si_3N_4/SiO_2/Si$ (TANOS) structures are compared with different gate voltages under the same thicknesses as shown in Fig. 8. Fig. 9 shows the program pulse of TATOS and TANOS structures with different gate voltages while the threshold voltage shift up to 5V. From the results we can see that the TATOS corresponds to higher speed due to the high-k materiel TiO_2 which causes higher electric field in the tunneling oxide as well as larger tunneling current.

IV. Conclusion

The memory performance of a novel TATHOS CTM device with the stacked HfO_2/SiO_2 tunneling layer and TiO_2 charge trapping layer are evaluated by a developed simulator. The effects of gate dielectric material and thickness, bias voltage and temperature are studied comprehensively. From the results we can see that appropriate stack structure for tunneling layer and a better choice for charge trapping layer could accelerate the program/erase speed and improve the retention characteristics simultaneously.

Acknowledgement

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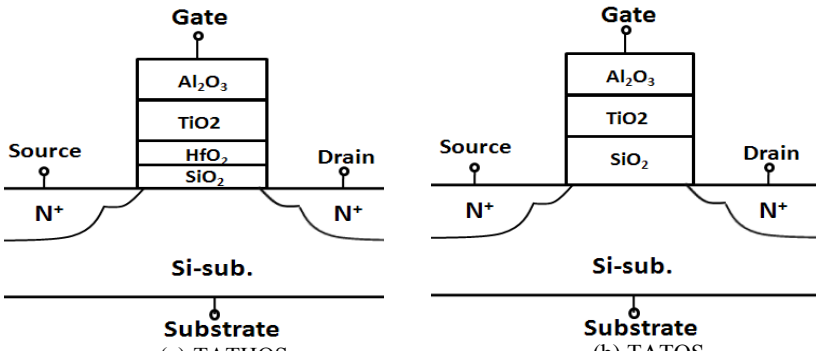
Reference

[1] Suhane. A, et al., *EDL*, pp. 396-398, 2010. [2] Soon-Moon Jung et al., *IEDM*, pp. 1-4, 2006. [3] G. Molas, et al., *IEDM*, pp. 22.5.1-22.5.4, 2010. [4] Lee.Chang-Hyun, et al., *Appl. Phys. Lett.*, pp. 073510-073510-3, 2005. [5] Hang-Ting Lue, et al., *IEDM*, pp. 1-4, 2009. [6] Hang-Ting Lue, et al., *IEDM*, pp. 547-550, 2005. [7] S. H. Lin, et al., *IEDM*, pp. 843-846, 2008. [8] Y.C.Song, et al., *SNW.*, pp. 1-2, 2008. [9] Y.C.Song, et al., *SISPAD.*, pp. 41-44, 2008. [10] Y. Park, et al., *IEDM*, pp. 29-33, 2006.



(a) TATHOS (b) TATOS

Fig. 1 The cross section of the TATHO(2)S, TATHO(1.5)S structure (a) and TATOS structure (b). Al_2O_3/TiO_2 thicknesses are 16/6.5nm for both (a) and (b). The tunneling layer EOT for TATHO(2)S , TATHO(1.5)S and TATOS is fixed to 4nm.

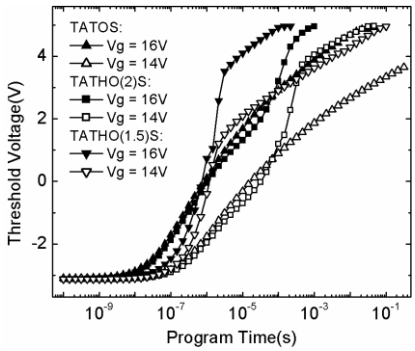


Fig. 2 The program processes of TATHO(2)S and TATHO(1.5)S are compared with that of the TATOS under different gate voltages.

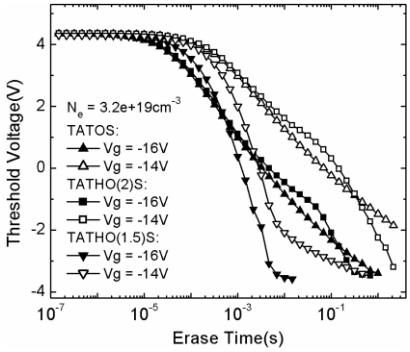


Fig. 3 The erase processes of TATHO(2)S, TATHO(1.5)S and TATOS structures under different gate voltages.

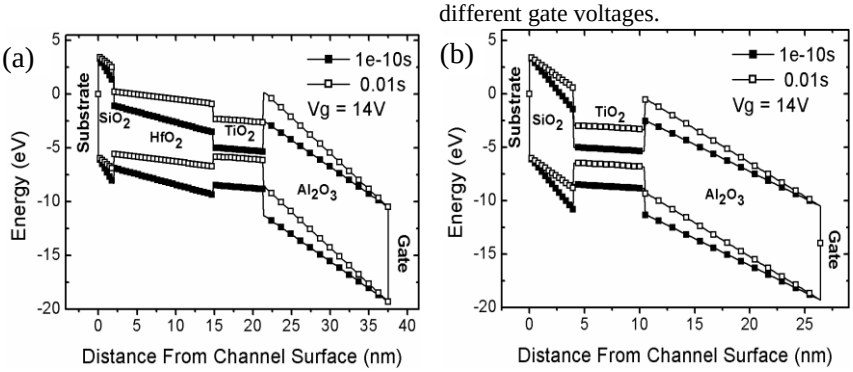


Fig. 4 The gate layers' electric potential variation during program performance with 14V gate voltage for TATHO(2)S (a) and TATOS (b) structures. The conduction band barrier between HfO_2/SiO_2 is about 2.15eV and 1.4eV between HfO_2/TiO_2 layers.

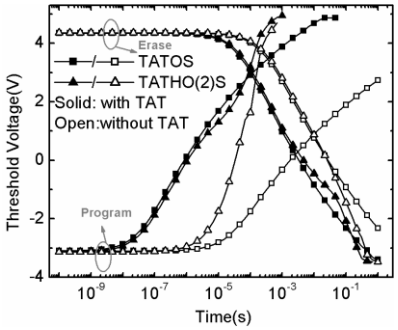


Fig. 5 The effect of TAT mechanism on program and erase performance based on the TATHO(2)S and TATOS structures.

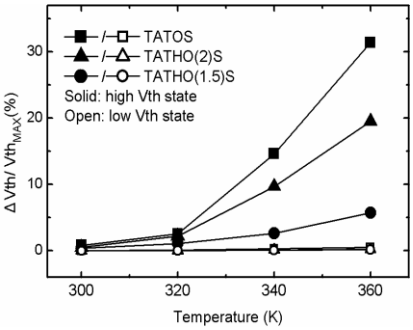


Fig. 6 Retention characteristics of high Vth state and low Vth state for TATHO(2)S, TATHO(1.5)S and TATOS structures under various temperatures while time up to 10^8s.

Parameter	Value
Φ_{TaN}	4.75 eV
σ_e/σ_h	$1\times10^{-13}/1\times10^{-13}$ cm^2
Φ_e	1.55 eV
Φ_h	1.4 eV
$m^*_{e,\,SiO2}$	0.42
$m^*_{h,\,SiO2}$	0.96
ε_{TiO2}	80
ε_{HfO2}	25

TABLE I The default parameters used in this work.

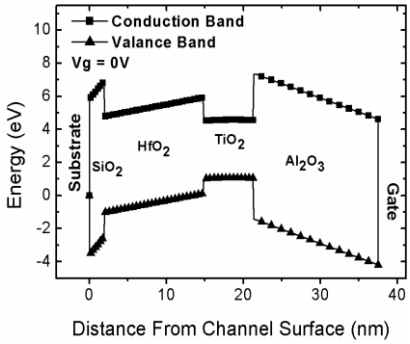


Fig. 7 Electric potential of TATHO(2)S structure' gate layers in retention performance with 0V gate voltage.

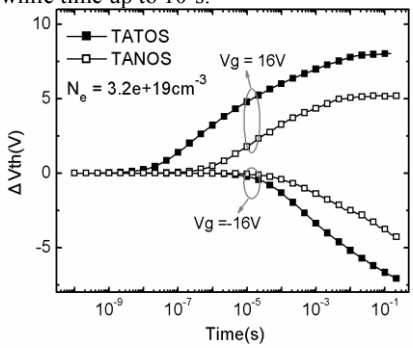


Fig. 8 The program and erase performance for TATOS and TANOS are compared with the blocking oxide/ trapping layer/tunneling oxide thicknesses are both 16/6.5/4nm.

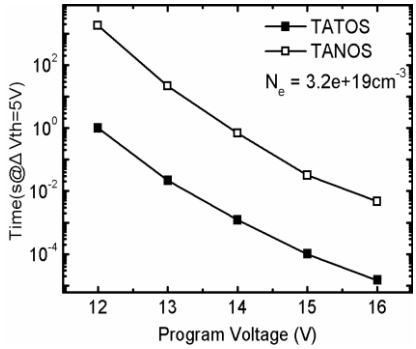


Fig. 9 The program time of TATOS and TANOS structures with 5V threshold voltage window under various gate voltages.