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The Research for Bulk Erase Operation in Vertical 3D Cell Array Architecture

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1. Introduction

3D memories have been focused for the future ultra-high density memory technologies to keep a trend of increasing bit density and reducing bit cost since 2D planar type memories have been faced with several device scaling limits. Recently several candidates of the technologies for the future 3D NAND flash cell array were proposed, such as BiCS[1], TCAT[2], 3D FG[3] and VG-NAND[4], to achieve aggressive scaling of the device dimension and terra-bit memory density.

Among them, BiCS and TCAT technologies have been focused as the promising candidates for terra-bit NAND flash memory, which can be replaced of the 2D NAND cell using floating poly-silicon. However, there are major concerns for each technology on the BiCS, TCAT flash memory. An erasing method using Gate Induced Drain Leakage (GIDL) for BiCS structure, and complicated process due to hard patterning of active area for TCAT structure have been concerned.

In this work, a novel cell array architecture, called "Bulk erasable-BiCS" is proposed to realize terra-bit memory density cell with electrode for bulk erase operation and competitive cell characteristics for the recent P-BiCS and TCAT from device simulation results. From this result, we expect that a bulk erasable BiCS technology using a flat plate erase electrode can be one of candidate structure for vertical 3D NAND flash memory.

2. Bulk erasable-BiCS Architecture and Key Features

Figure 1 shows the schematic of Bulk erasable-BiCS flash memory using bulk erase operation. In this structure, the additional poly-Si gates electrode is inserted in the middle of vertical string NAND cells, which gives a bulk erase operation. Since the erase operation of conventional BiCS Flash memory is done by hole current, which be generated by GIDL, there are several problems such as difficulty of time control between GIDL current and boosting voltage, and degradation of insulator on the lower select gate transistor. To solve these problems, we proposed Bulk erasable-BiCS structure with additional p+ poly-Si gate for bulk erase operation as shown in Fig. 1. Therefore, the conventional bulk erase operation can be achieved by applying substrate bias on the additional gate electrode during erase operation. This structure can be easily realized by an additional p+ poly-Si pattering after formation of bottom cell string. After p+ poly-Si formation, top cell string is performed. The separated channel formation is typical due to contact process issue with high aspect ratio.

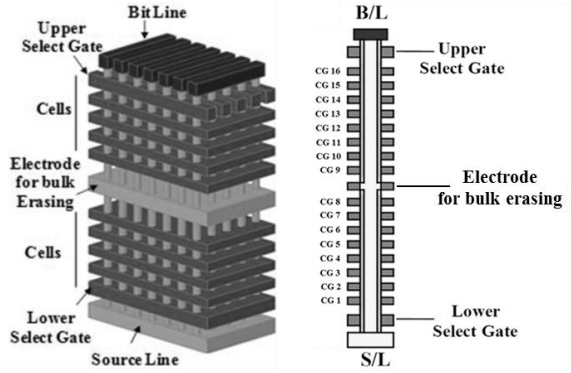

Fig. 1 (a) Schematic of Bulk erasable-BiCS Flash Memory with bulk electrode

The important key features are briefly indicated. Here, the diameter of poly-Si channel and gate length are 70 nm and 30 nm, respectively, and thickness of the tunnel oxide/nitride/block oxide (ONO) layer as a storage sites were selected to 6 nm/8 nm/3 nm. The poly-Si gate and channel being doped 1×10^{20} and 1×10^{15} Boron atoms/cm^3.

3. Simulation Result and Discussion

It is that achieved that transfer characteristics and wide P/E window are confirmed by Sentaurus TCAD simulation I_d-V_g as shown in Fig. 2 and 3, respectively. The program characteristics of the bulk erasable-BiCS flash cell arrays are shown in Fig. 2. Here, programming shows over 4.2 V at 1ms under a bias of V_{pro} = 20 V. Figure 3 Erase characteristics of the bulk erasable-BiCS flash cell arrays are shown in Fig. 3(a) and 3(b). Here, erasing shows under -1.5 V at 10 ms under a bias of V_{era} = 20V. Among them, erase simulation data of threshold voltage in several cells among 16 cells after bulk erase operation.

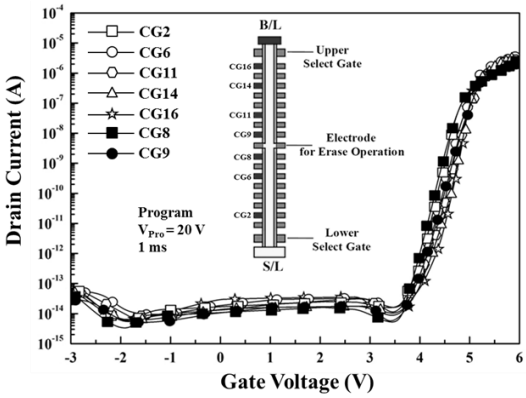

Fig. 2 The I_d-V_g characteristics of each memory cells after programming

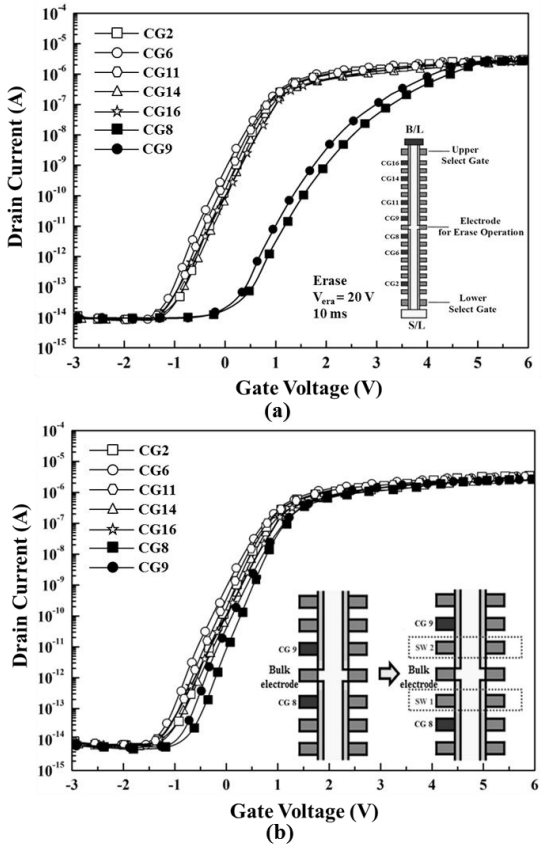

Fig. 3 The I_d-V_g characteristics of a direct coupling effect between adjacent cell and bulk electrode. (a) with switching Tr. structure. (b) without switching Tr. structure

Here, 8'th and 9'th cells are adjacent to bulk erase electrode. As shown in this Fig. 3 (a), threshold voltage for two adjacent cells has a different level showing under-erasing. We think that this degradation results from direct coupling effects due to high electric field between control gate of 0 V and bulk erase electrode of 20 V. In order to suppress this direct coupling, we propose the shielding-switching Tr. structure of 30 nm. As a result, Fig. 3 (b) shows these cells recovered to the same level of other cells. From this result, it is confirmed that control of cells adjacent to bulk erase electrode is very important.

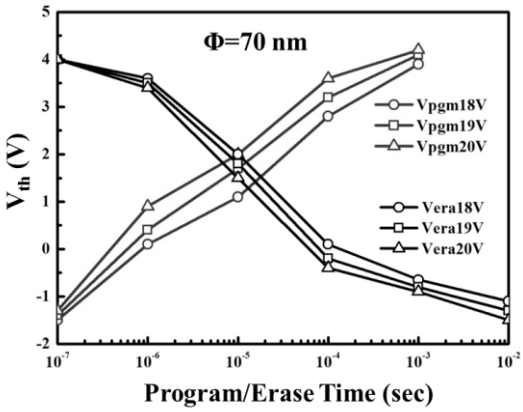

Fig. 4 Program/Erase characteristics of bulk erasable-BiCS NAND Flash Memory with various bias conditions.

During erase operation, 20 V is applied to an additional erasing electrode instead of source line. Using these conditions, we investigated the program and erase speed for variable program/erase voltages as shown in Fig. 4. Here, programming shows over 4.2 V at 1 ms under a bias of 20 V and erasing also shows under -1.5 V at 10 ms under a bias of 20 V, which are competitive to TCAT technology using bulk erase operation[2]. Furthermore, It is confirm that a wide shift of the threshold voltage of program and erase cell occurs at the low bias condition, which is that the program bias is as low as V_{pro} =18 V and erasing of the cell is obtained around V_{era}=18V as shown in Fig. 4

4. Conclusions

The novel structure of bulk erasable-BiCS NAND flash memory using bulk erase operation is proposed, and investigated for each memory cell characteristics. The bulk erasable-BiCS NAND flash memory has been successfully developed and the result shows wide P/E window of about 6 V. Furthermore, we confirm that bulk erasable-BiCS flash structure provides significant improvement in cell operation speed and variation of threshold voltage in erase state and enables Multi bit cell operation and Triple bit cell operation through electrode for bulk erasing. From these results, the bulk erasable-BiCS NAND flash memory could be a promising candidate for the future 3D NAND flash memory architecture.

Acknowledgements

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