Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp164-165

Inductorless Wideband Low Noise Amplifier with Variable Gain in 65nm CMOS

Dyg. Nur Salmi Dharmiza bt Awg. Salleh[1,2], Hiroyuki Ito[1], Noboru Ishihara[1] and Kazuya Masu[1]

[1]Solutions Research Laboratory, Tokyo Institute of Technology,
4259-S2-14 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan.
Phone: +81-45-924-5031 E-mail: paper@lsi.pi.titech.ac.jp
[2]Faculty of Engineering, UNIMAS,
94300 Kota Samarahan, Sarawak, Malaysia.
E-mail: asdnsdharmiza@feng.unimas.my

1. Introduction

Today, multistandard RF chips are in high demand for multipurpose wireless applications which fuels up research in wideband RF circuits. In RF circuits, the LNA plays an important role in determining the receiver's performance. However, despite of the CMOS technology scaling, passive devices such as inductors and capacitors that are commonly used for wideband circuits still consume large chip area [1].

This paper presents a variable gain wideband LNA with 3 gain modes that employs two bandwidth expansion techniques to achieve a large bandwidth without using inductors. Fabricated using the 65nm CMOS process, the LNA attains wide flat bandwidth of up to 3.8 GHz, 5.7 GHz, 7.8 GHz with gain 17.5 dB, 10.0 dB, and 0 dB for high-, middle-, and low-gain mode, respectively. The measured minimum NF during high-gain, middle-gain, and low-gain mode are respectively 4.0 dB, 7.3 dB, and 13.8 dB. Power consumption of this LNA is 13.8 mW at 1.2 V. The LNA core circuit is as small as 0.0121 mm^2 since no large passive device is used. Compared with other variable gain LNA from previous works [2][3], this LNA has good performance for wideband applications with smaller area.

2. Variable Gain Inductorless LNA

The proposed variable gain LNA adopted Cherry-Hooper and inverter-based negative feedback techniques [4] for bandwidth expansion. Cherry-Hooper technique achieves wide bandwidth by cascading amplifiers with appropriate mismatch and reducing Miller effect that usually limits the bandwidth [5]. Specification for the variable gain LNA is divided into three gain modes; high gain, middle gain, low gain, whereby gap for each mode is assumed to be about 10 dB from the range 0 dB to 20 dB. Fig. 1 shows the schematic of the variable gain LNA.

This LNA adopted an active peaking technique by using CMOS inverters as negative feedback to improve the bandwidth while at the same time achieves 50Ω input matching. This is quite challenging since we need to make sure that all three gain modes have good input impedance matching with required gain. This is realized by choosing different size of transistors for feedback inverters (M5~M12) using the mode switches. High and middle gain mode shares the same inverter size to achieve impedance matching while low gain mode uses half of the size.

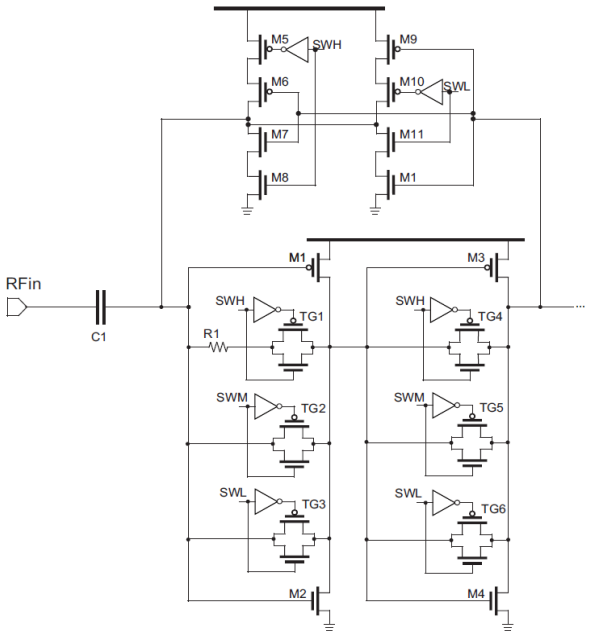


Fig. 1 Variable gain LNA schematic

At the front of the LNA, C1 is added as a DC blocking capacitor to prevent DC energy from flowing through sensitive RF components. Therefore its value is carefully chosen to be as small as possible while keeping the circuit to operate within the required frequency band.

Table I Gain control switch conditions

Gain mode	High gain	Middle gain	Low gain
SWH	ON	ON	ON
SWM	OFF	ON	ON
SWL	OFF	OFF	ON

Gain control for each mode is operated by using control switches (SWH, SWM, and SWL) that switch on and off complementary switches (TG1~TG6). As the complementary switch is turned on, on-resistance of the switch will become parallel resistor in the main amplifier stage. This therefore reduces the overall feedback resistance and hence affects the amplifier gain. Table I describes the condition for each mode.

3. Fabrication Results

The variable gain LNA was fabricated in triple-well 65nm CMOS process for validation. The chip micrograph is shown in Fig. 2. With this design, the circuit core only consumed 0.035×0.035 mm^2 excluding the DC block capacitor and buffer. With a 1.2 V supply voltage, the power consumption of the variable gain LNA was 13.8 mW for any gain mode.

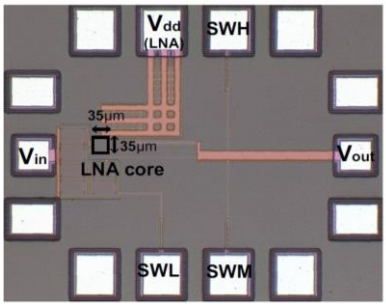


Fig. 2 Chip micrograph

Post-layout simulation results are compared with measurement results as shown in Fig. 3(a). From S21 results, the maximum flat bandwidth obtained for high-gain mode decreased from 7.6 GHz during simulation to 3.8 GHz due to a significant drop around 2 GHz of operating frequency. This might be due to wire line parasitic impedance on the circuit layout and transistor device mismatch. Simulation result shows 18.5 dB of gain, and measurement result has maximum gain of 18 dB.

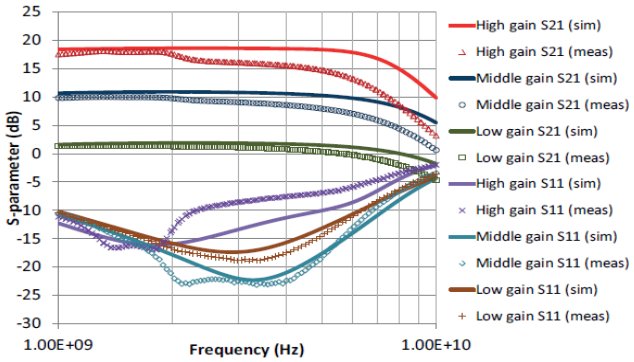
Meanwhile, S-parameter results for middle- and low-gain mode show similar trend with simulation results. Maximum flat bandwidth for middle-gain mode is 5.7 GHz, and bandwidth for low-gain is 7.8 GHz with input matching for both modes exceeded 5 GHz. Gain for both modes during simulation and measurement is almost identical with less than 1 dB difference.

Measured NF points were compared with post layout simulation results as shown in Fig. 3(b). From the results, high-gain mode achieved minimum noise figure of about 4 dB, while minimum NF for simulation results was 3.8 dB. As for middle gain mode, measured NF was above 7.3 dB and simulation results show minimum NF of 6.6 dB. Lastly, LNA in low-gain mode shows NF degradation from 12 dB during simulation to 13.8 dB when measured.

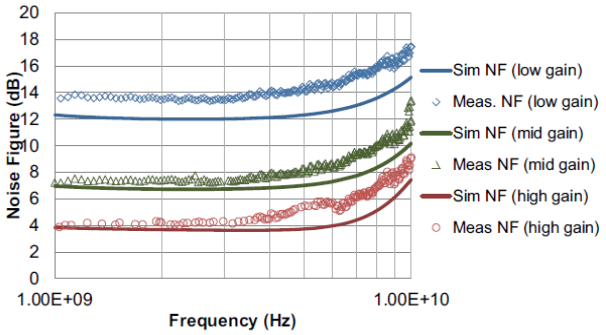
For linearity measurement, two-tone test was performed to obtain third-order input in-tercept point (IIP3). The IIP3 value for each high-gain, middle-gain, and low-gain mode was -23.9 dB, -16 dB, and -9 dB respectively with input tones of 1.995GHz and 2.005GHz.

4. Conclusions

Variable gain low-noise amplifier with three-step gain mode was proposed and fabricated in 65 nm CMOS process. From the results, 3-dB bandwidth for high gain mode dropped almost half from the simulation results, but other measurement results match fairly well with



(a) S-parameter results



(b) NF results

Fig. 3 Measurement and post-layout simulation results

simulation. This proves that the proposed gain control switch configuration to change the feedback resistance value succeeded in realizing a wideband LNA with variable gain function.

Acknowledgements

This work was partially supported by STARC, MIC. SCOPE, JSPS.KAKENHI, and VDEC in collaboration with Agilent Technologies, Cadence Design Systems, Inc., and Mentor Graphics, Inc.

References

[1] A. Matsuzawa,"RF-SoC expectations and required conditions," IEEE Trans. Microw. Theory Tech, Jan. 2002.

[2] C. Feihua, et al, "A CMOS Variable Gain LNA for UWB Receivers," J. Semicond. 32, 2011.

[3] C. Wang, et al, "A CMOS 2-11 GHz Continuous Variable Gain UWB LNA," IETE Journal, 2010.

[4] D. N. S Dharmiza, et al, "An Inverter-Based Wideband Low Noise Amplifier in 40nm Complementary Metal Oxide Semiconductor", JJAP, April 2012.

[5] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," IEE Proc., Feb 1963.