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ESD Protection Design for V-band Low-Noise Amplifier Using RF Junction Varactors

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1. Introduction

Electro-Static Discharge (ESD) protection is of extreme importance to modern RFIC design, especially with advanced technology node and high operating frequency. The shallow-trench-isolation (STI) diode is commonly used for RF Electro-Static Discharge (ESD) protection owing to the lower parasitic capacitances compared with the ggNMOS [1]. One approach to reduce the total parasitic capacitances is by using a diode string. However, it has been reported that the total ESD-induced parasitic capacitance cannot be reduced proportionally with the number of diodes [2]. Also, the increased trigger voltage with the diode string could be an issue for effective ESD protection. Compared with the Silicon Controlled Rectifier (SCR), also a very popular ESD protection scheme [3], the STI diode in general shows a drawback of intrinsically higher on-resistance. A polysilicon SCR was proposed with improved Q-factor and reduced signal loss, which is suitable for RF ESD protection design [4]. However, it can only be implemented in SiGe BiCMOS technology instead of a standard CMOS technology.

In this study, a different approach using the RF junction varactors as ESD protection is adopted. The varactor functions as a diode with a small on-resistance to conduct current, and provides excellent ESD protection. However, using the RF junction varactor as the ESD protection requires special design considerations compared with conventional RF circuits. By characterizing with high current *Transmission Line Pulse* (TLP) measurements, the optimized geometry of a junction varactor (L= 0.15 μm, W= 2 μm, and N= 25) can achieve the best figure-of-merit (FOM= V_{ESD}/C_{ESD}) up to 98.1 (kV/fF). The obtained RF junction varactors are then employed to realize an ESD-protected low-noise amplifier (LNA) at 60 GHz (V-band). This ESD-protected LNA demonstrates a 1.4-A TLP current level, corresponding to an over 2-kV Human-Body-Model (HBM) ESD protection level. Also, the LNA achieves a power gain of 16.5 dB and a noise figure of 6.6 dB at 60 GHz under a power consumption of 28 mW in 65 nm CMOS.

2. RF Junction Varactor for ESD Protection

The RF junction varactor is usually employed as voltage-dependent tunable capacitors in VCO designs [5]-[6]. The capacitance-tuning ratio (C_{max}/C_{min}) of a varactor directly correlates to the VCO frequency tuning range. The junction varactor can be used in the reverse bias mode of operation as an RF passive capacitor, and in the forward mode as an RF ESD diode. The two most important parameters, on-resistance and failure current of the ESD protection devices, are largely determined by the device layout and metal routing. For ESD protection, the junction varactors must be able to sustain a large current during ESD zapping. It is essential to have sufficient vias and a large metal width in both anode and cathode to prevent the electron-migration issue. Fig. 1(a) illustrates the cross-section view of the finger-type junction varactor with the structure of parallel connected p-n junction in N-Well. Fig. 1(b) shows the corresponding layout view of the customized RF junction varactor. Compared with the single-finger topology, the distributed multi-finger junction varactor has a large perimeter-to-area ratio, which shows enhanced ESD performance with relatively smaller parasitic capacitance. In addition, multi-metal-layer interconnection between anode and cathode has been employed to sustain a high ESD current without electron-migration.

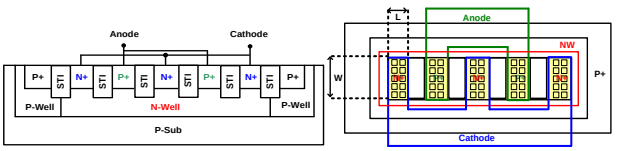
The TLP testing is often used to characterize the ESD robustness of the devices, which generates a pulse with a 10-ns rise time and a 100-ns width to simulate the HBM ESD condition. The secondary breakdown current It_2 is determined by a sudden increase of the leakage current. The relation between the TLP second breakdown current (It_2) and the HBM ESD level (V_{ESD}) can be approximated as V_{ESD} (V) ~ It_2 (A) · R_{HBM} (Ω), where R_{HBM} (= 1.5 kΩ) is the approximate equivalent resistance of the human body. The ESD bypass current capability of the junction varactors is investigated by varying the device finger width (W= 1 and 2 μm) and finger number (N= 25 and 50). The minimum device length of 0.15 μm, limited by the design rule, is selected for maximizing the total periphery. Table I summaries the corresponding ESD characteristics.

3. ESD-Protected LNA using Junction Varactor

Fig. 2 shows the circuit configuration of the proposed LNA with the complete ESD protection network. The LNA employs a two-stage cascode topology. The inductive source degeneration (L_S) is used for simultaneous noise and power matching, which forms the input matching with L_{G1}, JV_T, and JV_B. Also, the inductive loads (L_{D1} and L_{D2}) are used for gain peaking. The capacitor C_{12} performs as the DC block between the two stages, and works together with L_{G2} and L_{D1} as the inter-stage matching. The inductor L_{D2} and capacitor C_{D2} are also utilized as the output matching network. The transistor size is determined by investigating the noise and gain characteristics as a function of finger width and bias. The dual-diode topology (JV_T and JV_B) is employed for the ESD devices at the RF input to provide the direct ESD current paths for the PD and NS modes. The power clamp

consists of RC (resistor R and MOS capacitor M_C) and inverter (M_P and M_N) to trigger the large NMOS (M_{ESD}), which provides a low-impedance path from VDD to ground and completes the ESD paths for PS and ND modes.

The ESD-protected LNA was fabricated in a 65-nm CMOS technology with a chip area of 0.52 × 0.7 mm^2, including the probing pads for on-wafer testing. The LNA operates from a 1.2 V supply and draws a current of 23 mA with power consumption of 28 mW. Fig. 3 shows the measured S_{11}, S_{21}, and noise figures (NF) of the LNA, respectively. The LNA presents a peak power gain of 16.5 dB, an input return loss of greater than 21 dB, and a NF of 6.6 dB at the center frequency of 60 GHz. The ESD testing was performed using the Barth 4002 TLP testing system. Fig. 4 shows the TLP I-V characteristics of four different testing modes (PD, PS, ND, and NS) for the ESD-protected LNA [6]. In the PD and NS modes, the ESD current goes through JV_T and JV_B, respectively. In the PS and ND modes, the TLP curves show an additional offset voltage compared with the PD and NS modes due to the power clamp. In all the four modes, the second breakdown current It_2 up to ~ 1.4 A can be achieved, corresponding to an over 2.0 kV HBM ESD level. Table II compares this work with other prior arts. This work demonstrates a 60-GHz LNA with excellent ESD protection level and NF under a very small power consumption compared with prior works, as can be seen in Table II.



(a) (b)

Fig. 1. The proposed RF junction varactor for ESD protection in multi-finger topology (a) cross-section view, and (b) layout view.

TABLE I
ESD CHARACTERISTICS WITH DIFFERENT DEVICE SIZES

	W	L	N	It_2	V_{ESD}	C_{ESD}	V_{ESD}/C_{ESD}
Unit	μm	μm	--	A	kV	fF	V / fF
W1N25	1	0.15	25	0.7	~ 1.0	10.9	91.7
W1N50	1	0.15	50	1.4	~ 2.1	21.7	96.7
W2N25	2	0.15	25	1.4	~ 2.1	21.4	98.1
W2N50	2	0.15	50	2.4	~ 3.6	47.9	75.2

TABLE II
COMPARISON OF THE PROPOSED LNAS WITH PRIOR WORKS

Ref.	This Work	[7]	[8]	[9]
Tech. (nm)	65	130	65	130
Freq. (GHz)	60	60	60	60
NF (dB)	6.6	8.6	6.1	8.8
Power (mW)	28	65	35	54
S_{21} (dB)	16.5	20.4	19.3	12
HBM (kV)	2	1.5	--	--

4. Conclusion

In this study, we proposed of using RF junction varactors as ESD protection and co-designed with a 60-GHz LNA. The LNA demonstrated a noise figure of 6.6 dB and a power gain of 16.5 dB with a 2.0 kV HBM ESD performance.

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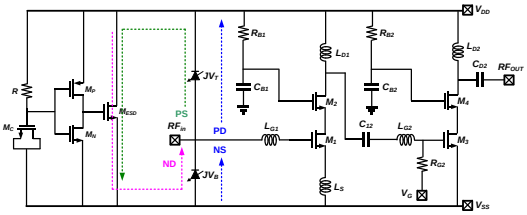

Fig. 2. Schematic of the proposed ESD-protected LNA.

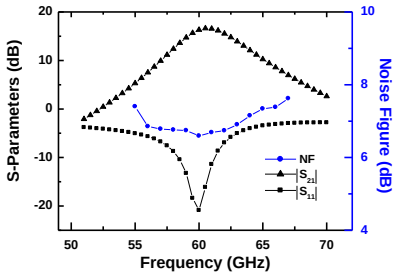

Fig. 3. Measured S_{11}, S_{21}, NF of the proposed ESD-protected LNA.

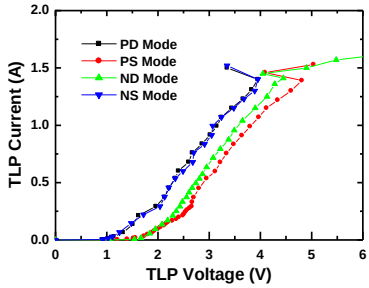

Fig. 4 Measured TLP *I-V* characteristics of the proposed ESD-protected LNA.