Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp168-169

A SIMPLE AND USEFUL LAYOUT SCHEME TO IMPROVE THE CDM ROBUSTNESS FOR THE INPUT BUFFER

Tzu-Cheng Kao [1,2], Jian-Hsing Lee [2], Chen-Hsin Lien [1], Chien-Wei Chiu [2] and Hung-Der Su [2]
1. Institute of Electronics Engineering, National Tsing Hua University, Hsinchu, Taiwan
2. Richtek Technology Corporation, Hsinchu, Taiwan

ABSTRACT

That the well pick-up density of the protected device has the great impact on the CDM ESD robustness of the input buffer is found. The less the well pick-up density, the higher the CDM robustness will be. This result also gives us a useful guide line to do the CDM improvement from the circuit layout once an IC cannot meet the required CDM level.

INTRODUCTION

It has been reported that the charged-device model (CDM) robustness of an IC strongly depends on the layout and function of the circuit and the package type [1]. However, the package type and circuit function are often not the items that could be changed. So, the only way the design house can do for CDM improvement is to revise the circuit layout. Except the interface circuit [2], however, what kind of circuit layout is susceptible to the CDM stress is still unknown until now.

From the comparison result of two different kinds of input buffers, the key layout parameter in terms of the CDM protection for input buffer is found. One input buffer only can pass CDM 150V, while another input buffer can pass CDM 1.5KV. Moreover, why the key layout parameter can affect the CDM robustness is found from the failure analysis result.

EXPERIMENT, ANALYSIS AND MECHANISM

The technology used to fabricate the chip for CDM study is a 0.4 um high-voltage (HV) 5V/12V BCD process. The oxide thickness for 5V device and 12V device are 100Å and 330Å, respectively. The circuit used for CDM evaluation in this production chip is an input buffer circuit as shown in Fig. 1. Except the HVN1, the transistors in the input buffer are all the 12V transistors with 12V gate oxides. The HVN1 is a 12V transistor with 5V gate oxide. The ESD protection device used to protect this input buffer is a grounded-gate 5V NMOS since the pad connects to the 5V gate oxide. Fig. 2 shows the layout of the ESD protection device, which is a multi-fingers device with the large contact to poly space on the drain.

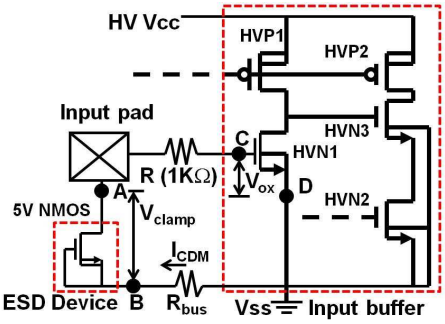

Fig. 1 Schematic diagram of the input buffer circuit.

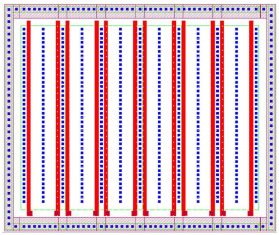

Fig. 2 Layout of the ESD device in Fig. 1.

A. Experimental Result

Fig. 3 shows the layout split for evaluating the influence of the well pick-up density on the CDM robustness of the input buffer. For input buffer IN-1 in Fig. 3a, the two HV N-transistors in Fig. 1 all have their own guard-rings. For input buffer IN-2 in Fig. 3b, the P+ diffusions of the two guard-rings to separate the two HV N-transistors are all removed except the top P+ diffusion. Table I shows the CDM test result. It can find that the well pick-up density can affect the CDM robustness of the input buffer significantly. The input buffer IN-1 with high density well pick-up only can pass +150V CDM and -150V CDM. However, the input buffer IN-2 with low density well pick-up can pass +1.5KV CDM and -1.5V CDM. Furthermore, the failure sides of the two input buffers after the CDM stress are definitely different, although both are the gate oxide damages at the transistor HVN1 (Fig. 4). The oxide damage site of the transistor HVN1 of the input buffer IN-1 is at the channel region, while it is at the overlap region between the gate and source for the input buffer IN-2.

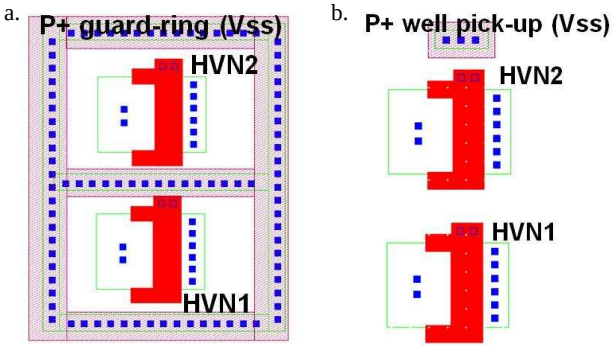

Fig. 3 Two different kinds of layouts for HV N-transistors in Fig. 1. a. IN-1, b. IN-2.

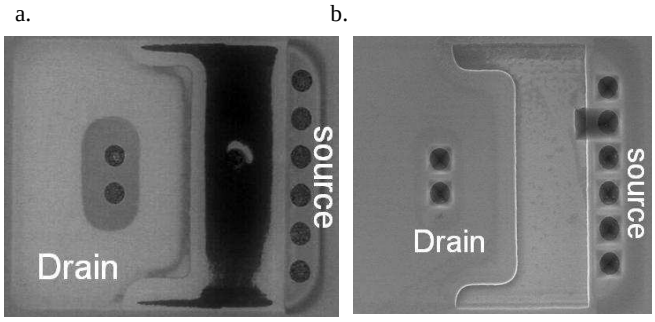

Fig. 4 CDM damage sties of HVN1 for a. IN-1, b. IN-2 in Fig. 3.

Table I : CDM test result vs. well pick-up density

Input Buffer	+CDM	-CDM
IN-1 (high density)	+150V	-150V
IN-2 (low density)	+1.5KV	-1.5KV

B. High Current IV characteristics

In order to investigate the ESD behaviors of the components in the input buffer, the high-current IV characteristics of the ESD device and 5V gate-oxide under the 1nsec fast transmission-line pulse (TLP) and 100nsec TLP are measured as shown in Fig. 5 and Fig. 6. The

ESD device can clamp the applied voltage of the 100nsec TLP stresses at 7V until its It2 (~3A), which is much smaller than the damaged voltage of the 5V gate-oxide (22V) as shown in Fig. 6. This is why the input buffer can pass 6KV human-body mode (HBM) zapping event even without the secondary ESD protection device. Apparently, the ESD device cannot clamp the applied voltage of the 1nsec fast TLP to a safe range, although it can sustain more than the 10A stress current. It can find that the voltage is increased to 30V at 6.5A and is clamped between 20V and 30V as the current is higher than 7A. For 1nsec fast TLP, the oxide damaged voltage of the 5V gate-oxide is nearly 29.5V (Fig. 6), which is below the clamped voltage of the ESD device. As the bus-line resistance is accounted (Rbus in Fig. 1), it will make the voltage across the oxide of the transistor HVN1 ($V_{ox}=V_{clamp}+I_{CDM}\times R_{bus}$) much higher than the oxide damaged voltage. This is why the CDM always induces the oxide damage at the transistor HVN1 of the input buffer in Fig. 1.

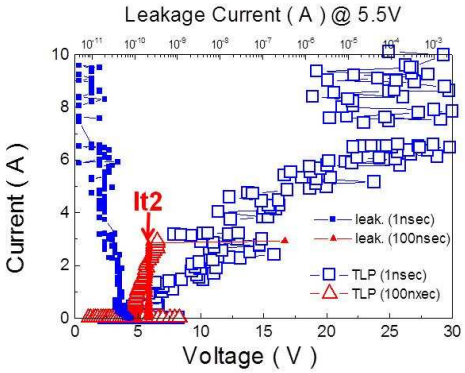

Fig. 5 High current IV characteristics of the ESD device in Fig. 2 under 1nsec TLP and 100nsec TLP stresses.

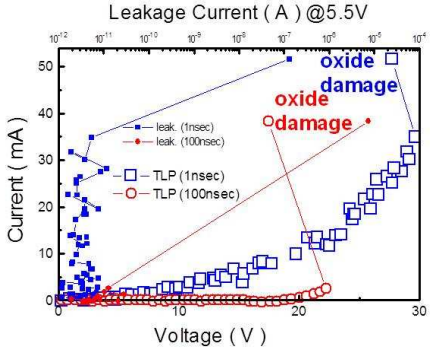

Fig. 6 High current IV characteristics of the 5V gate-oxide under 1nsec TLP and 100nsec TLP stresses.

C. Failure Mechanism

Fig. 7 shows a packaged IC chip under the CDM test [3], which is upside-down on a charged plate. The charge plate potential is raised to the setting voltage to charge up the voltages of all capacitors within the packaged IC [4] and then a grounded pogo pin is lowered to contact with a pin of the IC. During discharge via the zapped pin, the bonding-wire and pin act as an inductor L since the CDM is a nanosecond pulse. Then, the stored charges on the capacitors find all possible connections of the substrate (substrate contacts –guard rings- to V_{SS}, via parasitic n-well junction diodes to V_{DD}) ultimately via the ESD device and protected device to the grounded pin [5] as shown in Fig. 8. So, the potential of Vss is pulled up to $V_{clamp}+I_{CDMVSS}\times R_{bus}$ as the discussion in the above section. Based on this result, the equivalent circuit of the transistor HVN1 under the CDM can be simplified to a RLC circuit as shown in Fig. 9. For a short-duration time pulse, the peak stress current of a RLC circuit can be approximated to V_{ESD}/R [6]. From Fig. 9, the change of the well pick-up density will change the well resistance R_{PW}, resulting in the different stress current through the gate oxide of the transistor HVN1. The higher the well pick-up density, the more the current flows through the oxide above the channel (Coxc). This is why the input buffer IN-1 only can pass 150V CDM and why the oxide above the channel of the transistor HVN1 is damaged as shown in Fig. 4a. On the contrary, it only induces few currents flowing through the oxide above the channel if the transistor HVN1 is designed with the low density well pick-up. Moreover, the R_{PW} resistance becomes higher than the source series resistor R_S. Compared to the current flowing through Coxc, more current can flow through the oxide between the source and gate Coxs. So, the damaged site of the transistor HVN1 for input buffer IN-2 is changed to the oxide between and source and gate as shown in Fig. 4b and it can sustain the higher CDM stress.

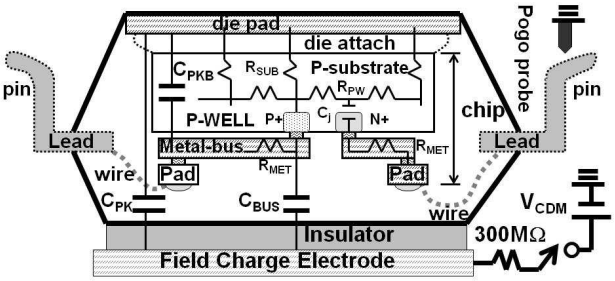

Fig. 7 Packaged IC chip under CDM test.

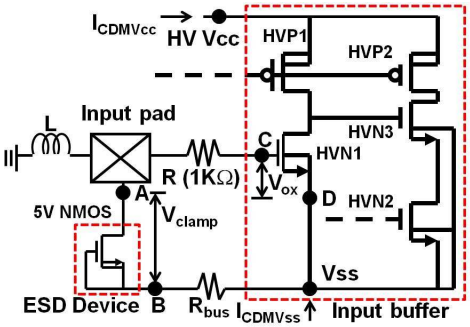

Fig. 8 Equivalent circuit of the input buffer in Fig. 1 under CDM test.

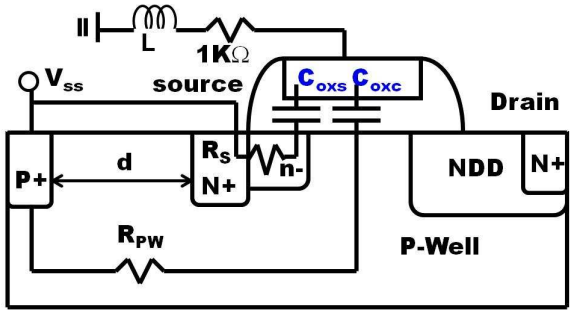

Fig. 9 Cross-section and equivalent circuit of the transistor HVN1 under CDM test.

CONCLUSIONS

Reducing the well pick-up density of the CDM sensitive circuit is a simple and useful layout scheme to improve the CDM robustness for an IC. Using this scheme, several productions are being revised and demonstrated that can achieve the required CDM robustness.

REFERENCES

[1] T. Suzuki et al., EOS/ESD sym., p. 325, 2008. [2] Eugene R. Worely, EOS/ESD sym, p. 238, 2004. [3] M. Etherton et al. EOS/ESD sym, p. 107, 2004. [4] J. H. Lee et al., IPFA, p. 228, 2009. [5] M. S. B. Sowariraj et al., IRPS, p. 608, 2005. [6] J. H. Lee at al., IRPS, p. EL. 2.1, 2012.