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A Ramp-wave Generator with Interleaved DACs for Single-slope ADC

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1. Introduction

The single-slope ADC, which is a component of the column parallel ADCs used in CMOS imagers, is well known as the simplest and smallest of the ADCs. When a ramp signal and an analog signal are given to a comparator, the comparator generates a PWM signal. The high-time of this signal is then counted by clock signal and the analog signal is digitized. The main disadvantage of single-slope ADCs is operation speed: whenever the ADC accuracy doubles, the operation time doubles as well and the power consumption thus increases. Various speed-up techniques have been proposed [1][2][3][4], but all require a high-speed ramp-signal generator.

In this study, we focused on the interleaved operation of DACs to achieve speed-up of the ramp-signal generator at a lower operation frequency.

2. Structure of the proposed circuit

2.1 Circuit composition of proposed circuit

Figure 2 shows a block diagram of the proposed circuit configuration. The circuit has three major parts. The first is a counter with multi-phase clock signals that are provided externally, and the second is a multi-stage current that steers the DAC unit. The current sources of the second part are p-MOSFETs for the lower bits and n-MOSFETs for the higher bits (Fig. 3). Outputs of the DAC units are merged and connected to the resistance. Final output is obtained by the voltage drop of the resistance with total current.

2.2 Circuit operation

Incremental digital input is given to four DAC units with quarter-clock phase delay and the outputs of the DACs are then summed. We denote four DAC outputs as a0, a1, a2, a3 and the quarter-clock phase delay of the DACs as z-1 in the Z-domain. The transfer function of the circuits is given by eq. (1):

$$H(z) = a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} \quad (1)$$

This function is equal to a 4th order moving average of the filter. When the stepwise signals at a clock period interval are given from the DACs, the moving average function is transferred to the DAC outputs and a stepwise signal can be generated at the resolution of a quarter-clock period. This means that DACs can generate high-speed signals based on the moving average function provided by the interleaved operation of the DACs. Moreover, since this circuit has some functionality, if the required wave form is simple, the circuit can generate a nonlinear signal such as a polygonal curve. To represent *n*-bit resolution by our circuits, we require 2^{n-m} DAC units with m-bit resolution and 2^{n-m}-1 sub bits. In this study, we set n = 12 and m= 4, respectively.

3. Simulation result

The proposed ramp-signal generator was designed and fabricated in TSMC 0.18-µm 1P6M CMOS technology. The layout is shown in Fig. 5. The total area (including four synchronous counters) was 0.5 × 0.25 mm2.

We simulated our circuits by using Cadence Spectre. Transient characteristics are shown in Fig. 6. The operation frequency was 200 MHz and the supply voltage VDD and output range were 1.8 V and 1 V, respectively. We confirmed that stepwise signals with a clock period were changed to the signal with a quarter clock period and that spike noise was reduced by four times (Fig. 6).

4. Experimental result

When a supply voltage of 1.8 V was given to our ADC, the operation frequency was 100 MHz and the DAC resolution was 10 bits. There were four DAC units. The entire DAC operated as one high-speed unit at 400 MHz with 12-bit resolution. It consumed 5.58 mW, including 1.44 mW by the counter and 4.14 mW by the DAC units. We characterized the static performance through an integral nonlinearity (INL) measurement. The INL was based on best fit line. In our ADC, a higher-order nonlinearity effect was observed. The measured INL was +/–0.7 LSB (Figs. 7, 8). The major causes of INL degradation were the clock jitter of the external clock signal.

5. Conclusion

We proposed a high-speed ramp-signal generator with an interleaved DAC that uses a multi-phase clock. The circuits we developed can achieve faster operation at a lower clock frequency. We designed and fabricated a 12-bit ramp-signal generator comprised of four 10-bit DAC units, and four 10-bit counters by using a TSMC 0.18-µm CMOS process. The circuit (at 12 bit, 100 MHz) was able to achieve an INL of +/–0.7 LSB. The entire generator consumed 5.58 mW with a 1.8-V supply.

Acknowledgment

This work was partially supported by SCOPE and by VDEC in collaboration with Cadence Design Systems, Inc.

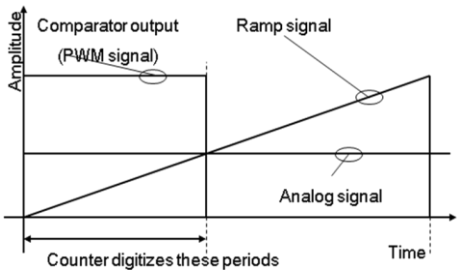


Fig. 1 Operation scheme of single-slope ADC.

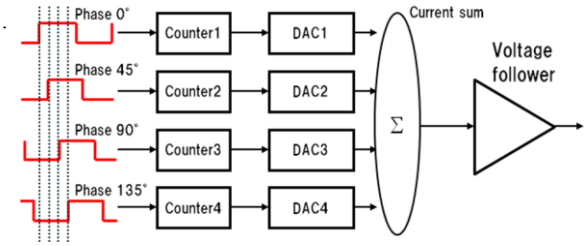


Fig. 2 Block diagram of proposed circuit.

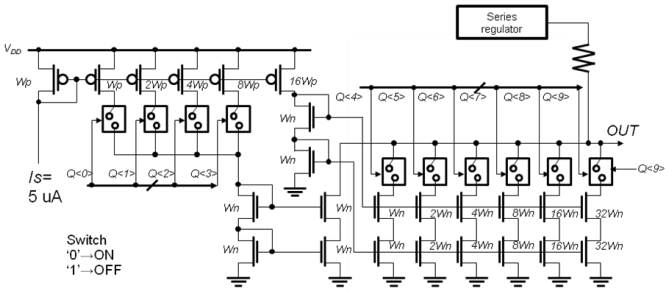


Fig. 3 Circuit composition of DAC unit.

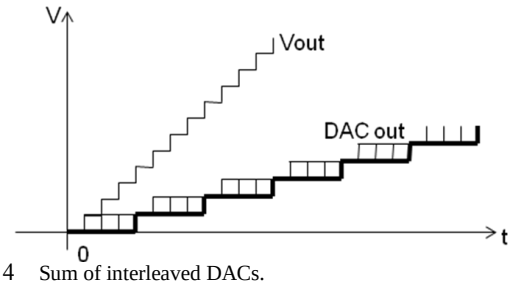


Fig. 4 Sum of interleaved DACs.

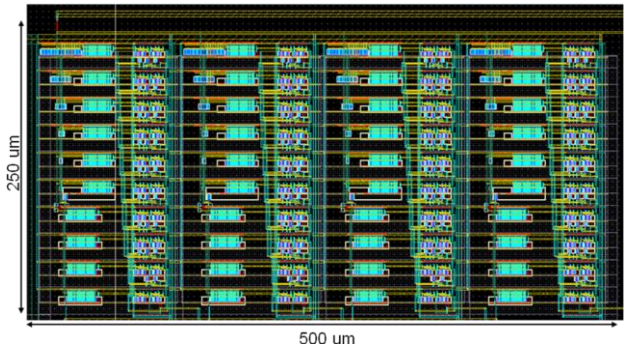
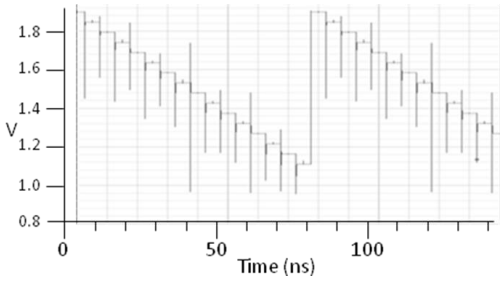
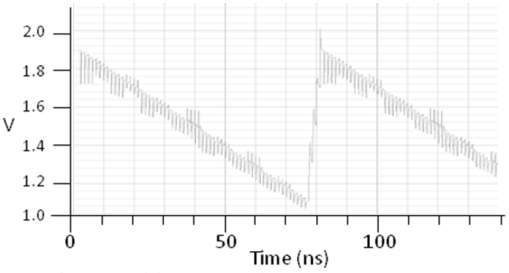


Fig. 5 Layout of our circuit.



(a) Output of single DACunit.



(b) Total output of four DACunits.

Fig. 6 Simulated transient characteristics.

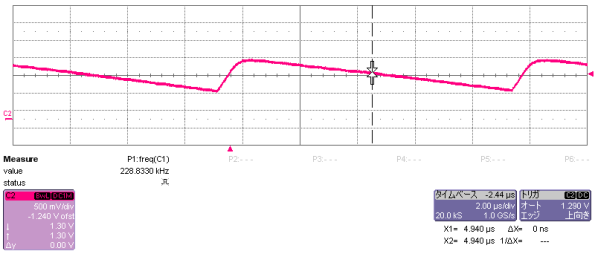


Fig. 7 Measured transient characteristics.

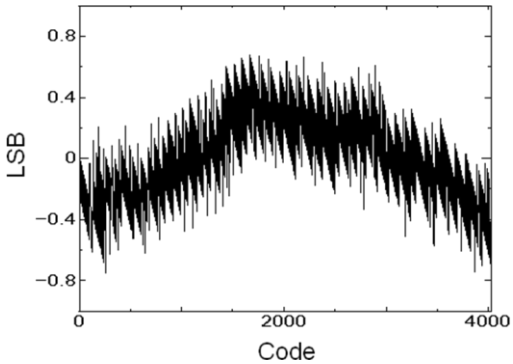


Fig. 7 Measured INL.

References

[1] S. Moong, et al., ICECS Proceedings, (2010) 863.
[2] Y. Nitta, et al., ISSCC Dig. Tech. Papers, (2006)27.5.
[3] T. Toyama, et al., ISSCC Dig. Tech. Papers, (2011)23.11.
[4] T. Takahashi, et al., VLSI symposia, (2011)90