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A 3-mW/Gbps 1.8-V Current-reuse LVDS Driver with 30% Power Reduction using Vertical MOSFETs

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1. Introduction

Recently low-voltage differential signaling(LVDS) drivers shown in Fig.1(a) with reducing the output swing voltage (V_{OD}) have been developed to reduce the power consumption[1]. However, when V_{OD} is too small, the receiver failes. Therefore, the current-reuse approach[2] reduces more effectively the power consumption keeping the output current I_{out} in proportional to V_{OD}. The basic current reuse driver is shown in Fig.1(b). It has two conventional LVDS drivers and two output port (U and D). Since the U-port current is reused in D-port, the power consumption is reduced to approximately half. However, it is still difficult to realize the low V_{DD} operation in this basic topology, because of the large voltage drops of cascaded MOSFETs.

To overcome the above problems, we propose a new topology for the current reuse LVDS driver. Moreover, we describe the proposed driver with the vertical MOSFETs and its excellent features, such as a power reduction with high data rate in low V_{DD} operation.

2. Circuit Design

The topology for the proposed current reuse LVDS driver is shown in Fig.1(c). The keys are: 1)cascaded current mirror with shared MOSFET, 2)vertical MOSFETs with body effect free[3]. Figure 2 shows the proposed current mirror in comparison with conventional one. The output current of the conventional decreases rapidly with V_{DD} falling. We design a new cascaded current mirror with shared MOSFET for our driver. Since the MOSFET(M_4, M_5) are shared with the current mirror and the switch cell(SW cell), the V_{DD} is reduced equal to V_S. Figure 3 shows the output current comparison. The output current decreasing from the ideal current I_M in our design is less than half the conventional. Figure 4(a) shows the structure of the vertical MOSFET[3] employed. Since the vertical MOSFET has no body-effect, and enables the low V_{DD} design compared with the planar MOSFET[2,3]. Figure 4(b) shows the voltage drop (V_n) of the circuit with cascaded vertical MOSFETs in comparison with conventional one. The voltage drop of the circuit(n=8) with the vertical MOSFET is 77.6% of that with planar one. Furthermore, we use the NMOS source follower in the down-side loop for stable operation.

3. Simulation Results and Discussion

We compare the characteristics of the following drivers; A, B, C and D. A shown in Fig.1 (a) is conventional driver without current reuse. B shown in Fig.1 (b) is basic current reuse driver with the conventional drivers. C and D shown in Fig.1 (c) are our proposed current reuse drivers. C is design with planar MOSFETs, and D is designed with vertical ones. In the simulation, we use the parameters of the 0.18-um planar MOSFET for 1.8-V in a 90nm technology. The vertical MOSFET is simulated with the model whose body is connected to the source. We set a target of V_{OD} as 200mV at 1.8-V V_{DD}. And, we set the mirror ratio as 40, and I_M (= $40I_B$) as 2.5mA for a V_{OD} target with a 100Ω R_L. Figure 5 shows the output voltage comparison between the drivers with and without the current reuse(A and D). The proposed design(D) shows the stable outputs as well as the conventional driver without current reuse(A). To compare the minimum operation voltage of each circuit, we define $V_{DD.OD}$, as V_{DD}, where a 200-mV V_{OD} is obtained. And we define $V_{DD.cmerr}$, with the feed-back error ($V_{cmd.err}$) equal to 10%. The minimum V_{DD} ($V_{DD,min}$) is defined as higher voltage of $V_{DD.OD}$ or $V_{cmd.err}$. Figure 6(a) shows the typical V_{OD} and $V_{DD.OD}$ of each driver, and Fig.6(b) shows the typical $V_{cmd.err}$ and $V_{DD.cmerr}$. Note that the U-port feed-back errors are small enough. The $V_{DD,min}$ of the A, B, C and D is 1.63, 2.39, 1.60, 1.45V relatively. The B-type with the conventional drivers can't be operated in low V_{DD}. Thanks to our proposed current mirror, the 1.8-V V_{DD} operation is achieved with enough margin in the proposed driver (C and D). Figure 7(a) shows the current reuse ratio η_R (=I_{out}/I_{toal}) of each driver. The C and D-types with our proposed topology show higher than 68% in the V_{DD} range from 1.4 to 2.6V. Figure 7(b) shows the power consumption P_{Normal} normalized by output power P_{out}. The P_{Normal} of the current reuse drive with two ports is given by

$$P_{Normal} = \frac{1}{2\eta_R} \cdot \frac{V_{DD}}{V_{OD}} \quad . \qquad (1)$$

Since each proposed driver (C and D) shows high η_R in low V_{DD}, the low P_{Normal} is achieved, though C (planar) is marginal with V_{DD} lower than 1.5-V. The proposed driver with vertical MOSFETs shows stable P_{Normal} with even low V_{DD}. The typical P_{Normal} of the proposed driver (D) is 5.3 with 1.8-V V_{DD} and 200-mV V_{OD}. This is equal to 70% of the conventional deriver (A) power. Figure 8 shows the achieved eye diagram of the proposed driver (D), with 1-ns data period, 1.7-V V_{DD}, 70ºC and SS parameters. The power consumption with 1.9-V V_{DD}, 0ºC and FF is 6.0mW. Thus proposed driver (D) with two ports achieves 2-Gbps with enough margins. The figure-of-merit is 3-mW/Gbps. The performance of our driver is summarized in Table I.

4. Conclusions

A low V_{DD} current reuse LVDS driver is proposed. The new cascaded current mirror and the vertical MOSFETs enable the stable V_{OD} and high η_R with low V_{DD}. The performance of 3-mW/Gbps with 1.8-V V_{DD} is achieved using parameters of a 0.18-um MOSFET in 90nm technology. Achieved power reduction is equal to 30% of the conventional driver power consumption.

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References

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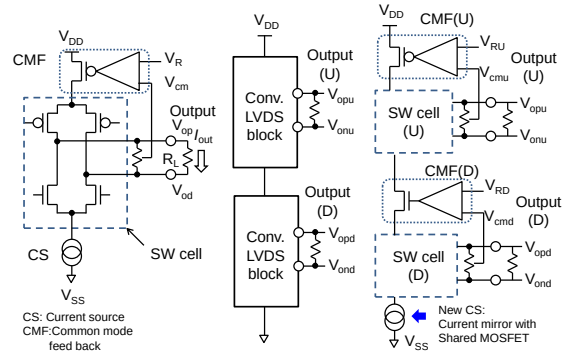
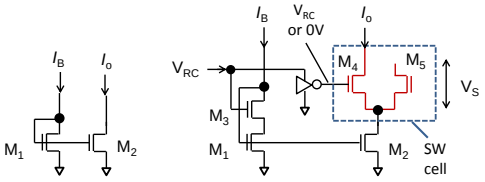


a)Conventional driver(A) b)Basic current-reuse driver(B) c)Proposed current-reused driver(C/D)

Fig. 1. Proposed LVDS drivers.



a)Conventional b)Proposed circ. with shared MOS

Fig. 2. Proposed Current mirror circuit.

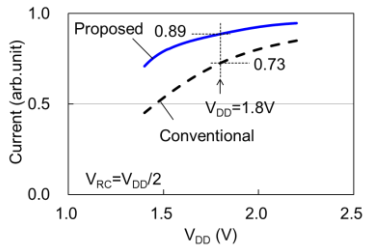
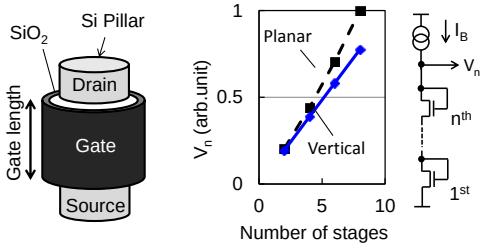
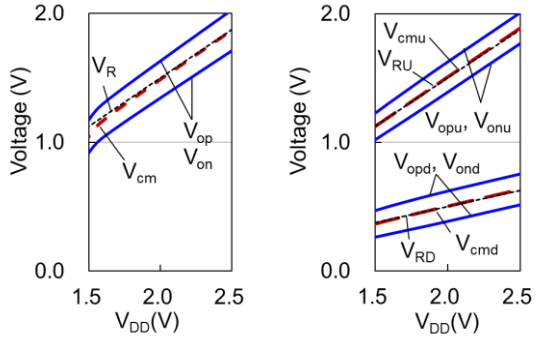


Fig. 3. Current mirror characteristics comparison.



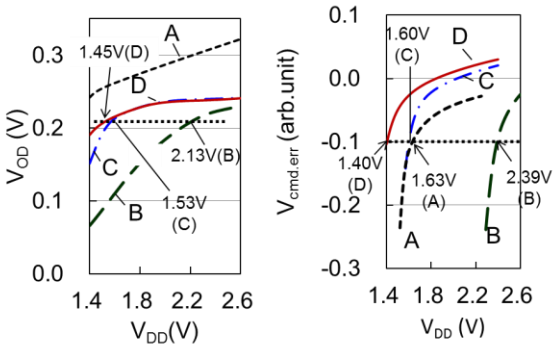
(a) Vertical MOSFET Structure[3] (b) Characteristics of circuits with cascaded MOSFETs

Fig. 4. Vertical MOSFET structure and characteristics of circuits with vertical MOSFTE in comparison with planar.



(a) Conventional driver(A) (b) Proposed driver(D)

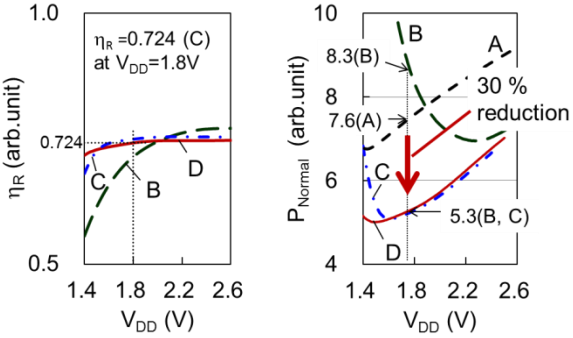
Fig. 5. Output voltage comparison.



(a) V_{OD} characteristics (b) $V_{cmd.err}$ characteristics

*A: Conventional t driver(planar),
B: Conventional basic current reuse driver(planar),
C: Proposed driver(planar),
D: Proposed driver(vertical)

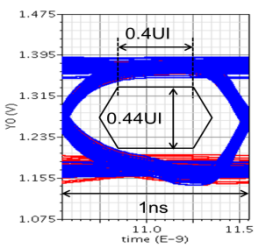
Fig. 6. V_{OD} and $V_{cmd.err}$ characteristics (I_M=2.5mA).



(a) η_R characteristics (b) P_{Normal} characteristics

*A,B,C and D: see Fig. 6.

Fig. 7. η_R and P_{Normal} characteristics (I_M=2.5mA).



*Load: L=2nH,
C_{L1}=0.2pF, C_{L2}=2.0pF.

Fig. 8. Eye diagram of the proposed driver (D).

Table I The proposed driver (D)

	min	typical	max	unit	Condition
V_{DD}	1.45			V	V_{OD}≥200mV, Tpical
V_{OD}	200			mV	V_{DD}≥1.7V, I_M=2.5mA, 70°, SS
D_{Rate}	2.0			Gbps	V_{OD}≥200mV, I_M=2.5mA 70°, SS
Pcir			6.0	mW	V_{OD}≥200mV, I_M=2.5mA, 0°, FF
ηR		0.74		au	I_M=2.5mA, Tpical
P_{Normal}		5.3		au	
P_{RED}		30		%	
V_{RU}=3V_{DD}/4, V_{RD}=V_{DD}/4, DRate:Total data rate of 2 ports					