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A Dynamic Comparator Using Dynamic Currents of CMOS Logic Gates for Low-Power and High-Efficient Offset Calibration

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1. Introduction

A comparator is one of the fundamental analog circuit building blocks, which compares an input voltage with a reference voltage, and outputs “High” or “Low” logic signals. They are widely used in various AD and DA converters. For comparators, an offset voltage, which is induced by mismatch between transistors, is one of the crucial issues and degrades the accuracy of the comparison. Thus, offset voltage calibration techniques for comparators are strongly required [1].

Several offset voltage calibration techniques have been proposed. For example, the techniques by pulling out some current from comparator with a current source [2] and adjusting load capacitances with capacitor banks were presented to cancel the offset voltage in the comparator [3]. However, the former increases the power consumptions due to the extra current source, and the latter increases area overhead due to the capacitors. Note that, although the capacitors are designed with MOS capacitor, the efficiency for the calibration is insufficient and the area will be increased.

In this paper, we propose an offset calibration technique that can provide high-efficient offset calibration with little area overhead. The technique we propose uses operating current of the logic gates to pull out the charge. The gates effectively pull out current from comparator for the calibration.

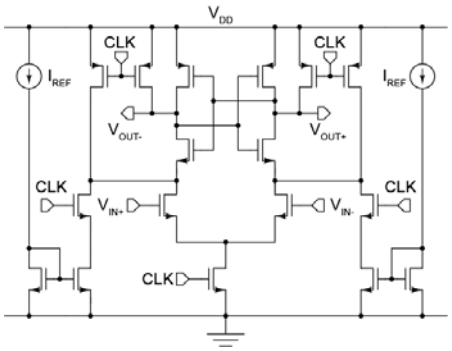

Fig. 1 Schematic of conventional dynamic comparator with offset voltage calibration circuit.

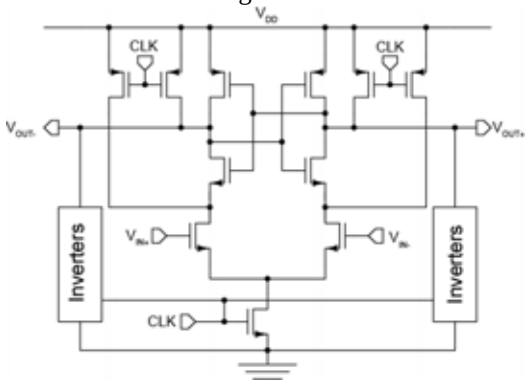

Fig. 2 Schematic of our proposed dynamic comparator.

2. Circuit Design

Figure 1 shows a schematic of a conventional dynamic comparator with an offset voltage calibration circuit [2]. In this circuit, the offset voltage can be calibrated by pulling out reference current I_{REF} from the comparator using the current source. However, the current source steadily dissipates the static power and increases power consumption. To solve the problem, we propose an offset calibration technique using primitive logic gates.

Figure 2 shows a dynamic comparator circuit with an offset voltage calibration circuit we propose. The circuit consists of the dynamic comparator and inverters as logic gates. The inverters are used to cancel the offset voltage of the comparator instead of using current source. The inverters operate when the comparator operates with the clock signal of CLK. Because the inverters dissipate dynamic operating current, we can use the currents for the calibration. By changing the number of inverters, we can calibrate the offset voltage of the comparator. Because the inverters dissipate large amount of operating current, the proposed offset voltage calibration technique can cancel the offset voltage of the dynamic comparator more effectively than other techniques.

Note that the impact of our calibration depends on the input pulse patterns. This is because the inverters’ current pulling out from the comparator varies according to the input pulse waveforms. When CLK (Low to High) is applied to the inverters, they dissipate only a short-current from the comparator. On the other hand, when CLKB (High to Low) is applied to the inverters, they dissipate both a short-current and a charge current from the comparator.

Figure 3 shows a whole block diagram of our proposed dynamic comparator. The circuit consists of the dynamic comparator, the inverters and a control circuit which includes logic circuits and registers. The calibration is performed by using a bit trial process similar to a successive approximation register (SAR). Sensing the offset voltage,

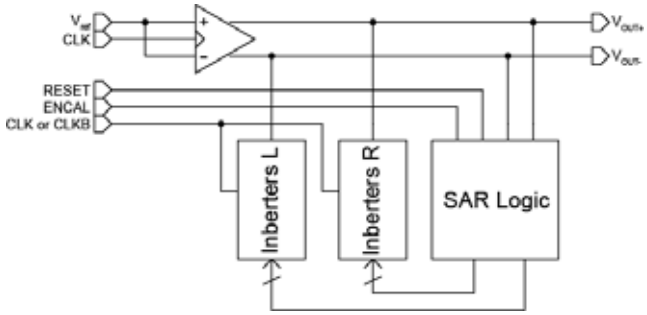

Fig. 3 Block diagram of our proposed offset calibration circuit.

both inverters do not operate at first. Next, the number of activated inverters in a group of inverters is decided by using binary search so as to cancel the offset voltage.

3. Results

The performance of the proposed circuit was evaluated with SPICE simulations using 0.18-μm CMOS process. The calibration using MOS capacitors was also investigated for comparison. All transistors were designed with the minimum size (L = 0.18 μm, W = 0.22 μm) in this technology. As previously explained, the current pulling out from the comparator depends on the input logic patterns. Therefore, we evaluated the circuit with different input logics (w/ CLK and w/ CLKB).

Figure 4 shows the calibrated offset voltage as function of calibration codes. The proposed circuits canceled the offset voltage in small calibration code. The required codes that calibrate 70-mV offset voltage are 7 (Prop. w/ CLKB), 15 (Prop. w/ CLK) and 255 (Conv. w/ C bank), respectively. Therefore, the proposed circuits cancel the offset voltage more effectively.

Figure 5 shows the energy consumption as function of the offset voltage. The proposed circuits dissipate lower energy compared with the conventional capacitor bank calibration.

Table I shows specification of our circuit and other circuit. Our circuit can operate in lower energy consumption than others.

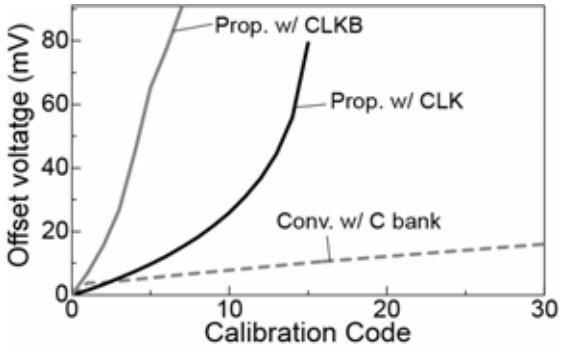

Fig. 4 Simulation result of cancelled offset voltage.

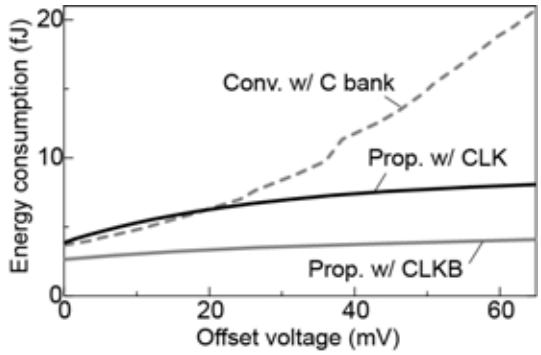

Fig. 5 Simulation result of Energy consumption.

Table I Specification of our circuit and other circuit.

Circuit	Process	Supply voltage	Frequency	Energy (@ offset)
Prop. w/ CLK	0.18 μm	0.5 V	1 MHz	3.9 fJ @ 0 mV 6.4 fJ @ 20 mV 7.5 fJ @ 40 mV
Prop. w/ CLKB	0.18 μm	0.5 V	1 MHz	2.6 fJ @ 0 mV 3.5 fJ @ 20 mV 3.8 fJ @ 40 mV
[4]	90 nm	1.0 V	3 GHz	54 fJ
[5]	65 nm	1.0 V	5 GHz	18 fJ
[6]	90 nm	1.2 V	3 GHz	71 fJ
[7]	90 nm	1.2 V	500 MHz	78 fJ
[8]	65 nm	1.2 V 0.6 V	7 GHz 700 MHz	185 fJ 67 fJ
[9]	90 nm	1.0 V	1 GHz	20 fJ

References

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