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A Low-Power Digital Baseband Processor for Passive UHF RFID Tag with Sensor and Sensor Interface

Shuangming Yu, Peng Feng, Weiyang Liu and *Nanjian Wu

State Key Laboratory of Superlattices and Microstructures,

Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, P. R. China

Phone/Fax: +86-10-8230-4754 E-mail: nanjian@red.semi.ac.cn

1. Introduction

Passive UHF RFID tags are widely applied in supply chain management, logistics, public transportation, and so on. If some sensors can be embedded or combined with the tag, the application area of the tag will be much extended [1, 2]. It is powered by harvesting RF electromagnetic wave energy from the reader. The lower power consumption the tag needs, the longer operation range it can support [3]. The power consumption of baseband processor with sensor interface occupies a large proportion of the whole RFID tag chip. Hence, one of the challenges in design of passive RFID tag with sensors and sensor interface is to reduce the power consumption of processor [4, 5].

This paper designs a novel low-power digital baseband processor for passive UHF RFID tag with on-chip sensor and interface for off-chip sensors. It integrates a power management block, on-chip sensor interface and I^2C-bus interface for off-chip sensors. It is fully compatible with the EPC C1G2 UHF RFID protocol. The power management block controls the operation of circuit blocks in chip adaptively. The I^2C bus provides an interface between the tag and off-chip active sensor. The baseband processor is fabricated in 0.18μm CMOS process. The area of the processor is 0.4×0.4mm^2. The processor consumes 7.9μW at 0.8V supply voltage and 1.1MHz clock frequency.

2. RFID Tag Architecture

Fig.1 shows the architecture of the passive RFID tag. It consists of RF analog frontend, digital baseband processor, non-volatile memory (NVM), on-chip temperature sensor and off-chip active sensor. The received signal is extracted from the antenna and demodulated by the RF analog frontend in the frequency range of 860MHz~960MHz. The baseband processor fulfills the process of protocol and controls the operation of sensors and NVM.

Fig.2 shows the proposed structure of the baseband processor. It receives the demodulated information from frontend, and then performs the decoding, CRC checking

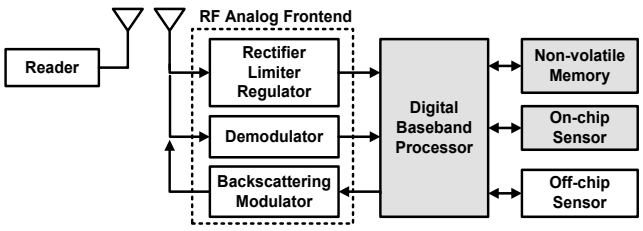

Fig. 1 Architecture of the passive RFID tag

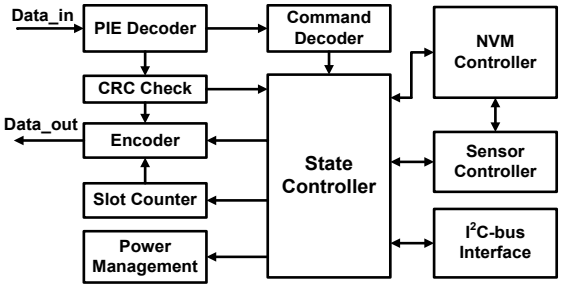

Fig. 2 Block diagram of the digital baseband processor

and command identification. Then it will start the NVM or the on-chip sensor or I^2C-bus interface block, according to the received command. Finally it sends message back to the reader. The processor employs Slotted ALOHA algorithm as anti-collision mechanism [6]. The power management (PM) block controls the operation of the circuit blocks in tag chip adaptively and dynamically so that the power consumption of the processor can be reduced effectively.

3. Design of Low-Power Baseband Processor

Fig. 3 illustrates the function of the PM block. It controls the operation of the circuit blocks in tag chip adaptively and dynamically. When the processor operates in receive state, only decoder and CRC check blocks are activated. After receiving the whole message, PM block disables the decoder and CRC check block, and enables command decoder and state controller. Then according to the received command, it will respectively start NVM controller or sensor controller or I^2C-bus interface and perform the read/write operation of the data. Finally, encoder and slot counter blocks are activated to encode the message and backscatter it to the reader. Thus, the PM block enables the operating blocks and disables the idle blocks dynamically to reduce the overall power consumption of the tag baseband processor.

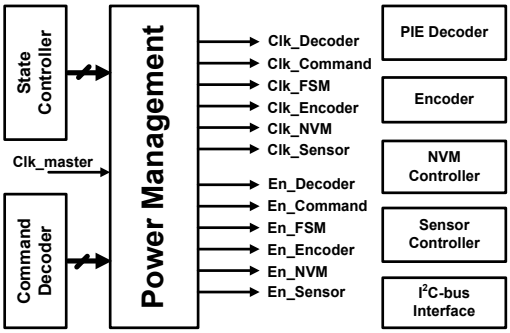

Fig. 3 Functional illustration of Power Management Block

As shown in Fig. 4, operand isolation and clock gating are used to reduce power consumption of the blocks. Operand isolation reduces the power consumption by eliminating unwanted transitions at the inputs of the combinational blocks. Clock gating reduces the switching activity of the sequential cells by turning off the clock signal. These techniques reduce the power consumption significantly.

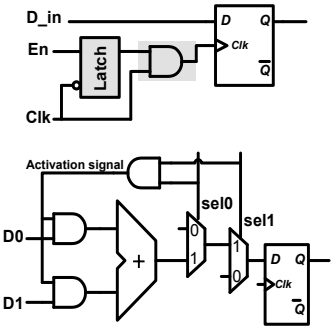

Fig. 4 Clock gating and operand isolation techniques

This processor can work properly with voltage from 0.8 to 1.8V. In order to minimize the power consumption, standard digital cells are selected to work at 0.8V. The power consumption is directly proportional to its clock frequency so that the clock frequency of the chip must be reduced as low as possible. We optimize the clock frequency of the chip by trading-off between the tag performance and the power consumption. Considering that the data symbol of uplink and downlink has a mid-symbol phase inversion, the minimum frequency should at least double frequency of uplink and downlink data rates.

4. Embedded Temperature Sensor and I²C-bus

A low power temperature sensor with dual-resolution operation modes: a high-resolution mode with a small temperature sensing range and a low-resolution mode with a wide sensing range, is embedded in the tag chip. The baseband processor controls the operation of the on-chip sensor. In specific applications, some other off-chip active sensors are also widely used, such as humidity sensor, acceleration sensor and so on. These sensors generally integrate I²C-bus interface to communicate with processor. In this design, I²C-bus interface block is designed in the processor to control the off-chip active sensor. I²C-bus interface can establish the correspondence between the tag and the off-chip active sensor. Thus, the RFID reader can access the off-chip sensor by operating the tag.

5. Measurement Results

The baseband processor was fabricated in 0.18μm CMOS process. The chip integrated a baseband processor, a dual-resolution temperature sensor, I²C-bus interface and 192-bit NVM memory. Fig. 5 shows the microphotograph of the chip. The area of the baseband processor is 0.4×0.4mm². We measured the chip. Fig. 6 shows that the baseband processor can correctly perform the EPC C1G2 UHF RFID protocol.

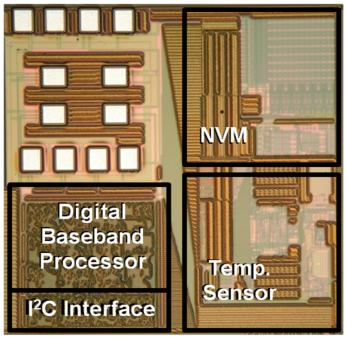

Fig. 5 Microphotograph of the RFID tag chip

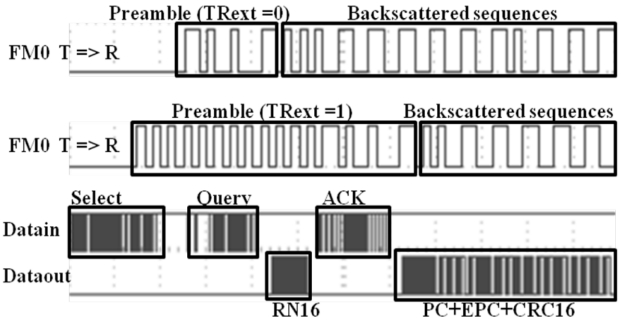

Fig. 6 Measurement results of baseband performance

The inaccuracy of the temperature sensor is -0.6˚C /0.5˚C (-1.0˚C /1.2˚C) over operating range from˚Ϭ to 15˚C in high resolution mode (-30˚C to 50˚C in low resolution mode). I²C-bus interface block is compatible with I²C-bus interface protocol. The baseband processor consumes 7.9μW at supply voltage of 0.8V and clock frequency of 1.1MHz.

6. Conclusion

This paper designed and fabricated a low-power digital baseband processor for passive UHF RFID tag with on-chip temperature sensor and interface for off-chip active sensors. It was compatible with EPC C1G2 protocol. The baseband processor consumes 7.9μW at supply voltage of 0.8V and clock frequency of 1.1MHz.

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