Investigation of trapping properties in AlGaN/GaN HEMT heterostructures grown on silicon with thick buffer layers

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1. Introduction

GaN based high electron mobility transistor (HEMT) heterostructures grown on silicon substrate are attractive due to their low cost, high power and high speed switching device operations [1,2]. However, the growth of high quality HEMT heterostructures is quite challenging mainly because of large thermal mismatch (~17 %) for GaN on silicon. As a result, large concentration of dislocation or defect arises which can eventually hamper hetero-interface transport properties. Moreover, the trap states near the hetero-interface can also limit their performance during rf applications [3]. Therefore, to overcome these challenges superior buffer layer design is essential for metal organic chemical vapor deposition (MOCVD) grown AlGaN/GaN heterostructures on silicon. In this work, we report on the improvements in AlGaN/GaN heterostructures and its interface properties by using multipairs of buffer layers.

2. Device fabrication

The AlGaN/GaN heterostructures were grown using Taiyo Nippon Sanso SR 4000 MOCVD system. The active device structure consists of AlGaN barrier and GaN layers with thickness of 25 nm and 1 µm respectively. The Al composition in the barrier layer was fixed as 26 %. To study the AlGaN/GaN HEMT interface properties an increasing sequence of AlN/GaN buffer layer thickness (T_{buff}) were used. The total epilayer thickness (T_{tot}) is given by the summation of GaN layer thickness (T_{GaN}) and T_{buff}.

Conventional device fabrication started with mesa isolation using BCl3 plasma based reactive ion etching. The devices were passivated using electron beam evaporated 100 nm thick SiO2. Ohmic patterns were performed using conventional photolithography followed by metallization of Ti/Al/Ni/Au (20/80/12/40 nm) metal stacks. The ohmic contacts were annealed at 850°C using infra-red lamp annealing for 30s in N2 ambient. Gate lithography was performed to define metallic Schottky gate. Finally, gate and contact metals Pd/Ti/Au (40/20/60 nm) was deposited followed by lift off procedures. Schottky barrier diodes of uniform area (7.07 x 10^{-4} cm²) were used for the conductance measurements.

3. Results and Discussion

The crystal quality of GaN layer with increasing T_{buff} were analyzed by measuring (0004) and (10-10) crystallographic reflections by high resolution X-ray rocking curve (HR-XRC) measurements using Philips X’pert x-ray diffractometer. The calculated screw dislocation density for AlGaN/GaN heterostructures with various T_{tot} was around ~1.5 x 10^{10} cm^{-2}. Meanwhile, the calculated edge dislocation density (D_{edge}) were found to decrease considerably with increasing T_{tot} and was low (≤52 %) for the heterostructures grown using thicker T_{buff} as shown in Fig. 1. The decrease in D_{edge} is attributed to the increase in T_{buff} which can overcome the large lattice mismatch between GaN and silicon substrate.

Low temperature (77 K) Hall measurements for these heterostructures yielded high carrier densities in the range of ~0.8 x 10^{13} cm^{-2} with an increasing carrier mobility (\mu_H) values for thicker T_{tot}. A plot of \mu_H measured as a function of T_{tot} is also shown in Fig. 1. As seen in the figure, the \mu_H was enhanced by 50 % for heterostructures grown on thick T_{buff} ~5 µm, compared to similar structures grown on thin T_{buff} ~1.25 µm. The increase in \mu_H reveals good quality AlGaN/GaN heterostructures relatively with a smoother hetero-interface and reduced D_{edge} in case of structures grown using thicker T_{buff}. A high concentration of dislocations/defects near the hetero-interface can ultimately limit the \mu_H due to interface roughness scattering (IRS) and/or dislocation related scattering [4].

![Fig. 1. Plot of calculated edge dislocation densities from XRC results and measured carrier mobilities versus total epilayer thickness for AlGaN/GaN HEMT heterostructures grown with increasing buffer layer thickness.](image)

Further, to quantitatively characterize the hetero-interface trapping properties frequency dependent conductance method was employed. Trap detection near the AlGaN/GaN interface or the channel is very much possible from conductance analyses by selecting gate voltages near the depletion [5]. Capacitance voltage (C-V) and conduct-
ance voltage ($G-V$) measurements were performed between frequency ranges (1 kHz-5 MHz) by sweeping the gate bias ($V_g$) using Agilent B1505 power device analyzer. The amplitude of ac signal was fixed as 20 mV and the measurement period was long enough, so that small signal conditions were maintained. A small negative shift in threshold voltage ($\Delta V_{th} \sim 0.12 V$) was observed on increasing the $T_{tot}$. To evaluate the trapping parameters, the equivalent parallel conductance/angular frequency ($G_p/\omega$) values near the depletion region were fitted to the equation (1) [5-7].

$$G_p/\omega = \frac{qD_t}{2\pi \tau_c} \times \ln[1+(\omega \tau_c)^2]$$

In this equation, the $D_t$ and $\tau_c$ are the trap state densities and trap state time constant that are evaluated by fitting the experimental $G_p/\omega$ values. As shown in Fig. 2, typical $G_p/\omega$ fitting curves against $\omega$ for selected gate voltages near the depletion region ($V_g < V_{th}$) showed an excellent agreement with the experimental $G_p/\omega$ results. Two kinds of traps namely slow and fast were evaluated for all the devices. The slow traps are surface related while the fast traps could be present near the hetero-interface or the channel as passivation had no effect on these traps [3].

![Fig. 2. Parallel conductance as a function of radial frequency at selected gate voltages near depletion region for AlGaN/GaN HEMT heterostructures with increasing buffer layers thickness. Solid lines represent the fitting curves of experimental $G_p/\omega$ values.](image)

The densities of slow traps ($D_s$) evaluated were in the order $\sim 0.5 \times 10^{12} \text{cm}^{-2}\text{eV}^{-1}$ with slow trap time constant ($\tau_s$) range between (0.3 – 1 ms). On the other hand, a decreasing trend in hetero-interface trap state density ($D_n$) with an exact exponential dependence of interface trap time constant ($\tau_n$) on applied gate bias was observed for the heterostructures grown with increasing $T_{buff}$. This signifies the presence of continuum of trap states near the channel as well as significant reduction in $D_n$ by improving the AlGaN/GaN heterostructures quality with thick buffer layers. A $D_{n-min}$ value of $2.5 \times 10^{10} \text{cm}^{-2}\text{eV}^{-1}$ was evaluated for AlGaN/GaN heterostructures grown with $T_{buff} \sim 5 \mu$m. In contrast, the $D_{n-min}$ value for similar heterostructures grown with thin $T_{buff} \sim 1.25 \mu$m was $1 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$.

4. Conclusion

The buffer layer thickness was increased in order to improve the quality of MOCVD grown AlGaN/GaN heterostructures on low cost and large area silicon substrate. Trapping properties near the interface were quantitatively characterized using frequency dependence conductance analyses. A slow $D_{s-min}$ value of $2.5 \times 10^{10} \text{cm}^{-2}\text{eV}^{-1}$ was evaluated for AlGaN/GaN heterostructures grown with $T_{buff} \sim 5 \mu$m against a $D_{n-min}$ value of $1 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ for similar heterostructures grown with thin $T_{buff} \sim 1.25 \mu$m. The interface trap time constants also revealed an exact exponential dependence against applied gate bias near depletion. Furthermore, the HR-XRC and Hall results also confirms that increasing the buffer layers thickness improves the AlGaN/GaN heterostructure and its interface properties as evident from reduced dislocation densities and enhanced carrier transport properties respectively.

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References