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Effects of Annealing Method on the Electrical Characteristics of Solution-Processed InGaZnO Metal-Point-Contact Transistor

Se-Won Lee, Yeong-Hyeon Hwang, and Won-Ju Cho

Department of Electronic Materials Engineering, Kwangwoon University, Seoul 139-701, Korea
Phone: +82-2-940-5163, E-mail: chowj@kw.ac.kr

1. Introduction

InGaZnO (IGZO) transparent amorphous oxide semiconductors have been studied for use as a channel layer in thin-film transistors (TFTs) and employed in such applications as active-matrix liquid crystal display and organic light emitting diode displays [1]. This is because that the IGZO shows better device performance than conventional hydrogenated amorphous Si TFT, with field effect mobility (μ_{FE}) below ~1 $cm^2/V{\cdot}s$. Recently, solution processed techniques such as spin coating and ink-jet printing has also been employed for the fabrication of a-IGZO based TFTs [2]. Major advantages of using the solution process include low production cost and high throughput with a simple process despite their poor electrical characteristics.

In this study, a novel TFTs structure, which has a metal-point-contact transistors (Ψ -MOSFET) structure without source/drain metal electrode, was proposed and investigated the effects of two-types of annealing method with solution-processed IGZO thin-film

2. Experimental details

P-type Si (100) wafers used as starting substrates and bottom-gate. Then, Si_3N_4 / SiO_2 (100 / 20 nm) staked gate dielectrics were deposited by using an RF magnetron sputtering system. A Si_3N_4 gate dielectric using buffer layer SiO_2 improve the channel / gate dielectrics interface and electrical instability [3]. The precursor solution of IGZO was prepared by dissolving 0.2 mol each of indium nitrate hydrate, gallium nitrate hydrate, and zinc acetate dehydrate in 20 mL of 2-methoxyethanol and then by mixing them with 0.1 mol monoethanolamine as a stabilizer. After removing solvents using oven in the 180°C for 10 min, the IGZO films were annealed under following conditions: a rapid thermal annealing (RTA) process and a conventional thermal annealing (CTA) process were carried out in the range from 200 to 600°C in N_2 ambient for 30 sec and in the range from 300 to 500°C in N_2 ambient for 30 min, respectively. The ramp-up rate and cool-down rate of RTA were kept to +30 and -20°C/s, respectively. The IGZO channel length and width are 80 and 20 um, respectively.

3. Results and Discussions

A schematic diagram of the conventional IGZO-TFT and the novel IGZO Ψ-MOSFET structures are shown in Fig. 1. Two tungsten probes were directly contacted on the IGZO channel layer in order to operate as a source and drain. The silicon substrate was contacted with the metal probe as the gate electrode.

Figure 2 shows the X-ray diffraction (XRD) and the scanning electron microscope (SEM) image of the IGZO thin film. Figure 2(a) shows the XRD patterns with regard to two-types of annealing method and various annealing temperature. Except for (100) Si peak at 56°, the sharp crystalline peaks were not found in any annealing process conditions, confirming the amorphous or nano-crystalline phase of the IGZO thin film. Figure 2(b) shows a surface morphology of the IGZO thin film with RTA, CTA, and post RTA (PRA) process. In the case of the RTA process, the IGZO film had a porous structure in which the grain size was approximately 10 nm.

Figure 3 shows the transfer characteristics (I_D-V_G curve) of the IGZO Ψ-MOSFET with the RTA and CTA process. Both RTA and CTA process devices not showed the transistor switching characteristics under 400°C due to imperfection chemical reaction of the IGZO film [4,5]. Compared to 500°C CTA device, the 600°C RTA device exhibited larger off-current, higher subthreshold swing (*SS*) value, negative turn-on voltage (V_{ON}) and larger drain current. Although the RTA process has a number of advantages such as short cycle time and low thermal budget, it also generate to mechanical stress between the IGZO channel and gate dielectrics due to fast ramp-up and cool-down speed. For this mechanical stress effect, the IGZO film suffered tensile stress from gate dielectrics owing to dissimilar coefficients of thermal expansion between the Si and the gate dielectric. Therefore, higher oxygen vacancy concentration can be expected due to lower vacancy formation energy for materials under tensile stress, and this corresponds to a more negative V_{ON}, and larger off-current [6].

Figure 4 shows the output characteristics (I_D-V_D curve) of the IGZO Ψ-MOSFET with the 600°C RTA and 500°C CTA process. Both devices present that the drain current increases linearly at low drain voltage and exhibits clear pinch-off and saturation of drive current at higher drain voltage.

Figure 5 shows the I_D-V_G curves of the IGZO Ψ-MOSFET with post annealing effects. The 500°C PRA process devices improved interface trap state (N_{it}) and decreased off-current because post CTA process alleviated mechanical film stress of the IGZO channel and gate dielectrics. Also, as shown SEM image of Fig. 2(e), the primary causes of device performance deterioration are not surface roughness of the IGZO film but thermal stress between the IGZO and gate dielectrics. The 500°C PRA process device especially showed the excellent electrical characteristics : *SS* value of 169.9 mV/dec, μ_{FE} value of 0.78 $cm^2/V{\cdot}s$, N_{it} value of 5.60 x 10^{11} cm^{-2}, and on/off current ratio of 5.34 x 10^6.

4. Conclusions

In summary, we investigated the electrical characteristics in the IGZO Ψ-MOSFET with two-types of annealing method. In the case of RTA process devices, the IGZO channel suffered tensile stress from gate dielectrics due to fast temperature change which cause thermal stress between Si and gate dielectrics. CTA process subsequent to RTA process devices exhibited improved performance in terms of lower *SS* value, higher μ_{FE}, and lower off-current because post CTA process alleviated mechanical stress of the IGZO and gate dielectric films.

Acknowledgements

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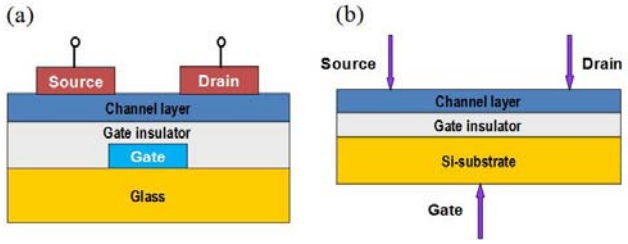

Fig. 1. (a) Schematic diagram of a conventional IGZO-TFT and (b) a novel IGZO Ψ-MOSFET structure

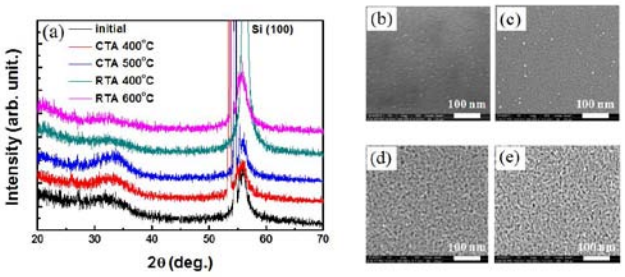

Fig. 2. (a) XRD patterns of the IGZO Ψ-MOSFET with annealing method and temperature. (b) SEM images of the IGZO film surfaces with the initial (c) 500°C CTA (d) 600°C RTA and (e) 500°C PRA process

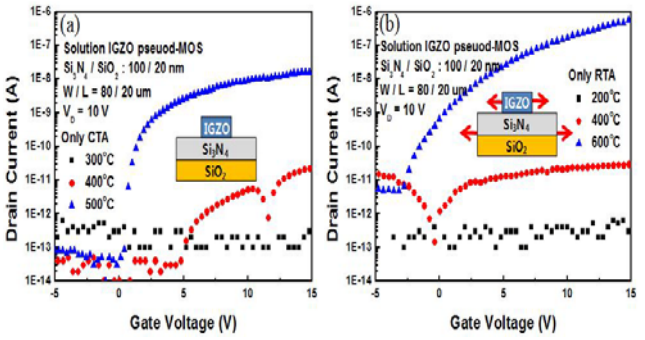

Fig. 3. Transfer (I_D-V_G) characteristics of the IGZO Ψ-MOSFET with two-types of annealing method and various temperatures. (a) The CTA process carried out ranging from 300 to 500°C. (b) The RTA process carried out ranging from 200 to 600°C. The inset of (b) shows the side-view of the IGZO and gate dielectrics with tensile stress

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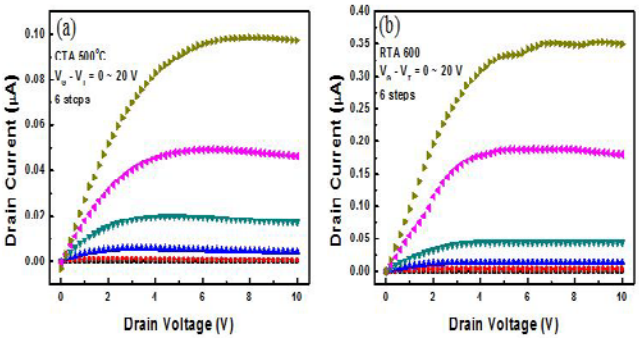

Fig. 4. Output (I_D-V_D) characteristics of the IGZO Ψ-MOSFET with (a) the 500°C CTA and (b) 600°C RTA process.

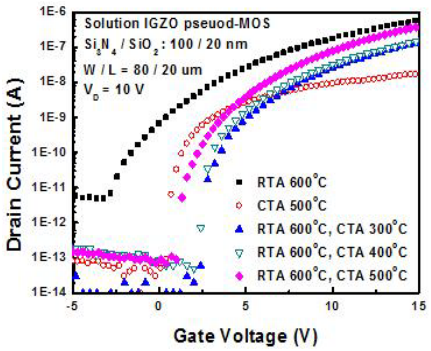

Fig. 5. I_D-V_G characteristics of the IGZO Ψ-MOSFET with the CTA, RTA, and PRA process at various temperatures.

Table 1. Various TFT parameters of the IGZO Ψ-MOSFET withthe CTA, RTA, and PRA process at various temperatures.

	V_{ON} (V)	*SS* (mV/dec)	u_{FE} ($cm^2/V{\cdot}s$)	I_{on}/I_{off} ratio	N_{it} (cm^{-2})
RTA only (600°C)	-2.82	848.88	0.78	1.05×10^5	4.75×10^{12}
CTA only (500°C)	0.37	162.41	9.8×10^{-3}	3.34×10^5	5.22×10^{11}
PRA 300°C	2.42	163.4	0.32	6.75×10^6	5.27×10^{11}
PRA 400°C	2.1	160.15	0.47	4.73×10^6	5.21×10^{11}
PRA 500°C	0.95	165.28	0.775	5.34×10^6	5.40×10^{11}