Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp210-211

Low Frequency Noise Analysis of ZnO TFTs under the Positive Gate Bias Stress

Kwang-Seok Jeong[1], Yu-Mi Kim[1], Ho-Jin Yun[1], Seung-Dong Yang[1], Sang-Youl Lee[1], Young-Su Kim[2], Hi-Deok Lee[1] and Ga-Won Lee[1]*

[1] Dept. of Electronic Engineering, Chung-nam National University, Yusung-gu, Daejeon 305-764, Korea
Phone: +82-42-821-5666 E-mail: gawon@cnu.ac.kr
[2] National Nanofab Center, Eoeun-dong, Yusong-gu, Daejeon, 305-806, Korea

1. Introduction

ZnO-based thin film transistors (TFTs) have attracted much attention for their applicability to flat, flexible, and transparent display devices [1,2]. In addition, high-mobility characteristics have indicated that these devices could play roles in both the driving device of AMOLED and the switching device of AMLCD [3,4]. Despite of these merits, the electrical stability of ZnO-based TFTs can be easily degraded, which has been reported due to the temporary charge trapping by diverse defects such as interface traps, oxide traps and grain boundary traps. This electrical instability in ZnO TFTs can be also caused by defect state creation within the ZnO channel under the bias [5]. However, most researches on the instability have been based on the common dc current–voltage (I-V) measurement. The I-V analysis is indirect and not sufficient to discriminate defects location and properties. In this paper, we have adopted the low-frequency noise (LFN, 1/*f* noise) analysis method to investigate the instability mechanism of ZnO TFTs under the positive gate bias stress. The 1/*f* noise analysis is known to be a powerful tool for defect studies and to the quality of the channel layer and technological process used to elaborate the structure [6,7].

2. Experiment

In order to fabricate ZnO TFTs with inverted staggered structures, a Ti gate layer of 100 nm on the SiO_2/Si substrate is deposited by RF magnetron sputter at room temperature. After the Si_3N_4 film of 200 nm is deposited as the gate insulator by PECVD at 150 °C, ZnO films as the channel layers are deposited by RF magnetron sputter at 100 °C, respectively. In this experiment, the channel layer thickness was varied to 20 nm and 80 nm to fabricate the devices with different instability properties. Next, the passivation layer, insulation film between the channel layers, and contact/metal pad are formed. Measurements were made on devices with a channel length of 20 μm and a width of 50 μm.

The constant positive gate bias stress in devices under test is applied by semiconductor parameter analyzer (4156C). The 1/*f* noise measurements are performed at room temperature using a dynamic signal analyzer (35670A) preceded by a low-noise current–voltage converter, a low-noise voltage amplifier (SR570), and Agilent 4156C.

3. Result and Discussion

Fig 1 is the I-V characteristics of the fabricated device A (20nm) and B (50nm) before and after stress. In case of device A, the electrical properties are worse before the stress but the amount of V_{th} shift after stress is smaller and recovered after relaxation time, which shows that the instability properties are different according to the active layer thickness. It may be because the process condition influences on the film quality. 1/*f* noise of device A and device B were measured under the gate bias stress voltage of 30 V and the stress and relaxation time of 10^4 at the fixed V_{DS} of 1.5 V. As shown in **Fig. 2**, the drain current power spectral density (S_{ID}) of both devices deviates from the ideal 1/f noise behavior (the exponent values in normal MOS device = 0.7~1.3), which can be explained due to deep traps at the grain boundaries near the interface [8]. **Figure 3** shows the normalized drain current power spectral density (S_{ID}/I_D^2) of both devices according to the gate overdrive voltage (V_{GS}-V_{TH}) after the gate bias stress and relaxation. The origin of 1/*f* noise can be discerned from the gate bias dependency. If the slope of S_{ID}/I_D^2 approached -1, it was known to follow the mobility fluctuation model which is closely related to the crystal quality of channel layer, while if it approached -2, it was following the number fluctuation model, which is induced by trapping/de-trapping of free carriers into the oxide trap sites near the interface [9]. The slopes of all devices fitted from 6 V to 15 V at a fixed frequency of 20 Hz are about -1. That is, the instability of ZnO TFTs can be related to traps existing in the channel layer. **Figure 4** shows α_{app} and V_B of both devices according to V_{GS}-V_{TH} after the gate bias stress and relaxation. Here, α_{app} can be used as a figure of merit to represent the grain boundary trap density and the height of the grain boundary potential barrier (V_B) in inhomogeneous materials like the poly-crystalline semiconductor [10]. α_{app} and V_B of both devices increases after the gate bias stress. As shown in **Fig. 4 (a)**, device A under relaxation recovers the original characteristics, which can be explained as the fact that the free carriers under the bias stress is trapped temporarily into grain boundary trap sites in channel layer and when the stress bias is removed, they are de-trapped out of grain boundary trap sites. However, in **Fig. 4 (b),** α_{app} and V_B of device B does not recover the initial properties under relaxation. This result is exactly in agreement with the transfer characteristics of **Fig 1.** In **Fig 5,** the electrical characteristics of both devices are summarized. In case of

device B, the sub-threshold slope (SS) are degraded under bias stress while SS of device A is almost invariable. From these 1/*f* noise as well as I-V analysis, the instability in device B is regarded to be the result of stress-induced created traps rather than pre-existing traps at or near the channel/gate oxide. It is also possible that the dominant charge trapping is in oxide not at the channel/gate oxide interface and grain boundary where carriers can be easily de-trapped without any thermal/bias annealing [5]. Moreover, as shown in **Fig. 6**, the charge injection into oxide is supported by smaller breakdown voltage (BV) of device B under stress than that of initial device B. That is, the reliability degradation of device B can be explained due to trap creation at interface between channel layer/gate oxide and charge injection into gate oxide.

4. Conclusions

In this paper, 1/*f* noise analysis is carried out in ZnO TFTs under the gate bias stress and relaxation varying channel thickness. The S_{ID} of both devices deviates from the ideal 1/f noise behavior, which can be explained due to deep traps at the grain boundaries near the interface. All devices follow the mobility fluctuation model, which can be related to traps existing in the channel layer. α_{app} of both devices according to V_{GS}-V_{TH} after the gate bias stress and relaxation is investigated. The device A under relaxation recovers the original characteristics, which is exactly in agreement with I-V measurement results. It means the temporary charge trapping at the grain boundary traps is dominant under the stress. However, α_{app} value and the transfer parameters of device B do not recover the initial values under the relaxation, and SS is dreaded after the gate bias stress. Moreover, device B under stress has smaller BV than initial device B. That is, the electrical reliability degradation of device B can be explained due to trap creation at interface between channel layer/gate oxide and charge injection into gate oxide.

Acknowledgements

This research was financially supported by Basic Science Research Program and the Human Resource Training Project for Regional Innovation through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (MEST) (20100028160).

References

[1] Yutaka Ohya, et al., Jpn. J. Appl. Phys. 40 (2001) 297. [2] J. H. Chung, et al., Thin Solid Films. 516 (2008) 5597. [3] R. B. M. Cross, et al., Appl. Phys. Lett. 89 (2006) 263513. [4] Sang-Hee K. Park, et al., Adv. Mater. 21 (2009) 678. [5] R. B. M. Cross, et al., Appl. Phys. Lett., 89 (2006) 263513. [6] S. Ju, S. Kim, et al., Appl. Phys. Lett., 92 (2008) 022104. [7] I.-T. Cho, et al., IEEE Electron Device Lett., 308 (2009) 828–830. [8] Hongki Kang, et al., Appl. Phys. Lett., 99 (2011) 062106. [9] P. Magnone, et al., IEEE Trans. Device and Materials Reliability. [10] Kwang-Seok Jeong, et al., IEEE Electron Device Lett. 32 (1701) 12.

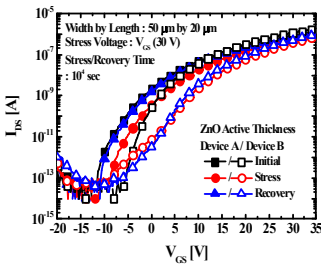

Fig. 1. Transfer characteristic curves of ZnO TFTs before and after stress, and under relaxation.

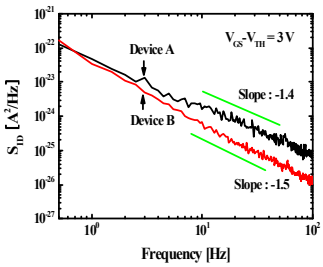

Fig. 2. S_{ID} according to frequency in ZnO TFTs.

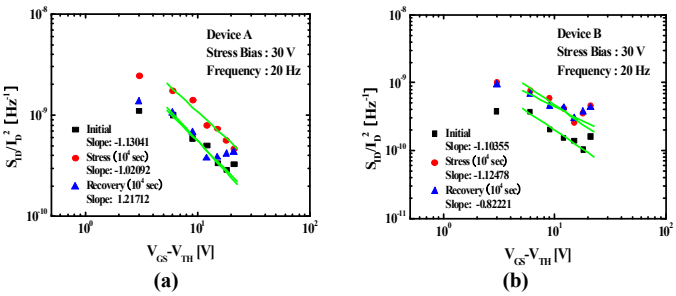

Fig. 3. S_{ID}/I_D^2 according to V_{GS}-V_{TH} after the stress bias of 30 V for the stress and relaxation time of 10^4 sec in ZnO TFTs.

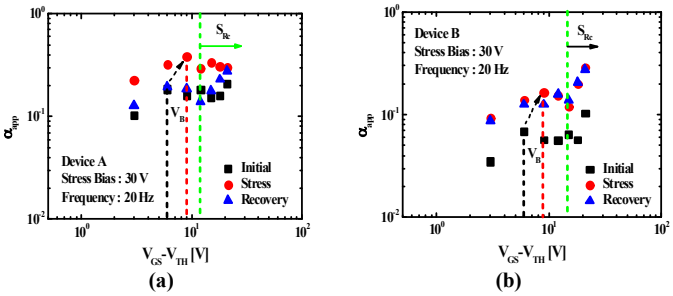

Fig. 4. α_{app} according to V_{GS}-V_{TH} under the stress bias of 30 V for the stress and relaxation time of 10^4 sec in ZnO TFTs.

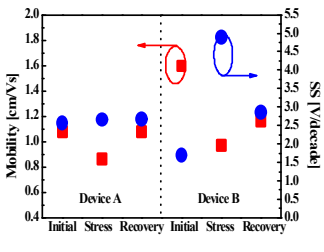

Fig. 5. Mobility and SS of ZnO TFTs before and after stress, and under relaxation.

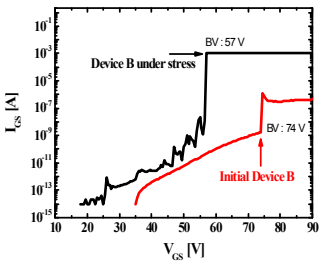

Fig.6. Breakdown voltage (BV) of device B under stress and initial device B