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Analysis on trade-off between electric field and gate-drain capacitance for GaN HEMT by T-CAD simulation

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1. Introduction

GaN features higher breakdown voltage, higher saturation velocity and better thermal conductivity compared with existing semiconductor materials of GaAs and Si. Therefore, GaN is becoming a major material for high power and high frequency microwave amplifiers. These days, GaN HEMTs (High Electron Mobility Transistor) with more than 100W output power and more than 60% PAE are available [1]. However, details of electronic trapping effect are still unknown. It sometimes causes degradation of power conversion efficiency and is one of serious problems. It is believed that strong electric field concentrated at the drain side edge of the gate electrode is the source of such electronic trapping effects. Therefore, so-called gate field plate (GFP) structure is often employed to reduce the maximum electric field (Emax) at the gate edge. By enlarging length of GFP, concentration of electric field can be relaxed [2]. However, it has a draw back of increased feedback capacitance (Cgd) and reduced gain. Therefore, trade-off between Emax and Cgd should be investigated quantitatively to optimize the device structure.

In this paper, Emax and Cgd are calculated by using T-CAD technology to show trade-off relation ship between them. It was found that there exists a knee point, beyond which Emax remains constant while Cgd continues to rise. Also efficiencies are calculated for various structures from the T-CAD results. It was found that power added efficiency exhibits highest value at that knee point.

2. Simulation of electric field and capacitance

In this work, Emax and small signal response at microwave frequency are calculated with T-CAD [3] for various GFP length structures. Also small signal equivalent circuit parameters are extracted from calculated small signal response. Bias conditions for calculating Emax is Vd=30V and Vg=-5V. Maximum electric field at 0.5nm underneath AlGaN/GaN hetero interface is defined as Emax. Small signal equivalent circuit parameters are extracted for conventional microwave FET model for Vd=30V and Vg=-2V [4]. Calculated Emax versus Cgd is shown in Fig.1. Only GFP length is varied for each point. As can be seen in Fig.1, there exists a structure C where best compromise between Emax and Cgd can be obtained. In Fig.2, calculated electric field along the AlGaN / GaN hetero interface is shown for structure group A and B. Structure group A, which has shorter GFP than structure C, features that Emax increases as Cgd decreases, as is shown in Fig.1.

This is because electric field that peaks at gate edge overlaps with electric field that peaks at GFP edge. as is shown in Fig.2(a). Meanwhile, Structure group B, whose GFP length is longer than Structure C, exhibits that Emax is kept constant while Cgd becomes larger as GFP is longer. This is because two electric fields , one that peaks at gate edge and the other that peaks at GFP edge, become independent each other, as is shown in Fig.2(b).

At GFP length of structure C, two electric fields shown above just start overlapping. Therefore, best compromise is achieved.

ATLAS simulator from Silvaco was employed for the calculation.

3. Calculation of power added efficiency (PAE)

To make sure that Structure C, which has the best compromise for Emax and Cgd, indeed exhibits highest efficiency, efficiency of the transistor is calculated for each structure. To calculate efficiency, it is very important to take into account the effect of drain resistance increase due to charging and de-charging of electronic traps under large signal RF operation. Drain resistance at RF operation, Rd_rf, is estimated as follows. Fig.3 shows measured pulse current (Vgq=-1V) versus calculated Emax. From Fig.3, it can be deduced that pulse current linearly changes with respect to Emax. This is because reduced Emax suppressed charge and de-charging rate. Assuming that Rd_rf linearly corresponds to pulse current, Rd_rf is calculated as a function of Emax. Then, by using Rd_rf and small signal equivalent circuit parameters, PAE for each structure is calculated according to the improved Raab's model [5]. This model is the Raab's model in which knee voltage and leak current is also considered. As shown in Fig.5, Structure C shows highest PAE, as was expected.

4. Conclusion

In conclusion, trade-off relationship between maximum electric field at gate edge and parasitic capacitance between gate and drain electrode is calculated with T-CAD. It was found that for certain gate field plate length, best compromise for low electric field and parasitic feedback capacitance is obtained. Calculating effective drain resistance under RF operation revealed that that optimized structure gives highest PAE also. It was found that optimization of gate field plate length was very important for an improvement of PAE.

References

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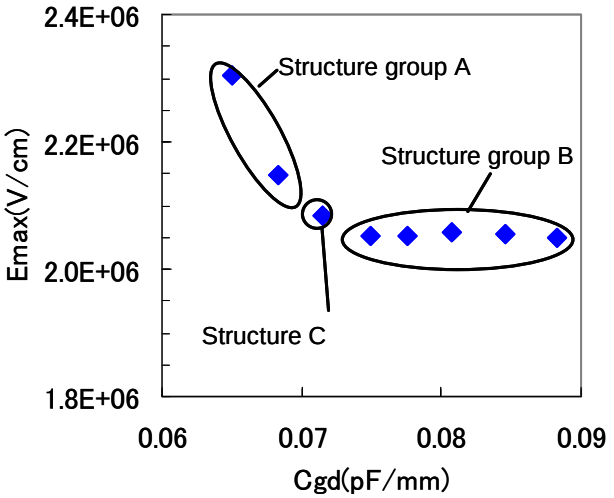
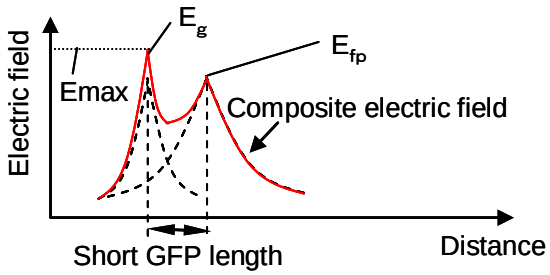
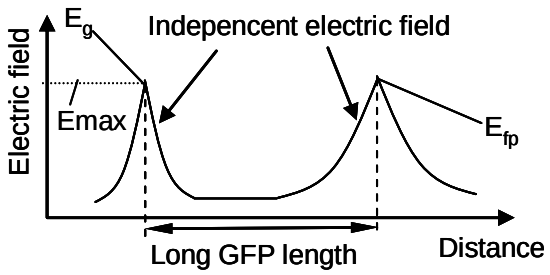


Fig. 1 Simulated maximum electric field near gate metal (Emax) and gate-drain capacitance (Cgd).



(a)



(b)

Fig. 2 Schematic electric field distribution (a) structure group A (b) structure group B. Eg and Efp are the peak of electric field at the edge of gate and gate field plate, respectively.

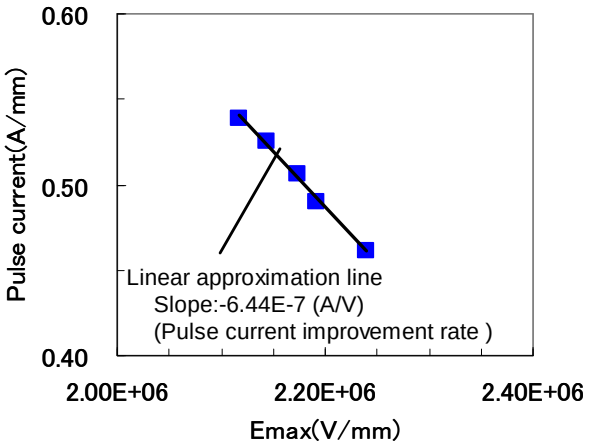


Fig. 3 Measured pulse current (Vgq=-1V) versus calculated Emax.

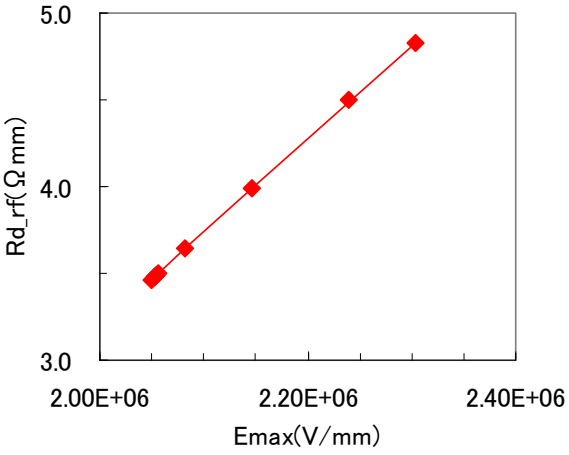


Fig. 4 Measured pulse current (Vgq=-1V) versus calculated Emax.

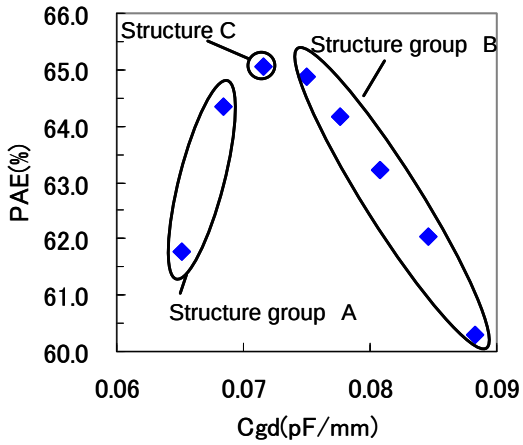


Fig. 5 Simulated maximum PAE and Cgd.