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Comparison of Noise and Power Characteristics of Single- and Dual-Gate AlGaAs/InGaAs pHEMTs

Chih-Chan Hu[1,2], Shu-Hsien Lin[2], Dong-Ming Lin[3], Chien-Chang Huang[4], Yue-Ming Hsin[2,*], Cheng-Kuo Lin[5], Yu-Chi Wang[5], Yi-Jen Chan[6]

[1] System Manufacturing Center, Chung-Shan Institute of Science and Technology
New Taipei 237, Taiwan
[2] National Central University
No.300, Jhongda Rd., Jhongli City, 320, Taiwan
[*] Phone: +886-3-4227151 ext. 34468 E-mail: yhsin@ee.ncu.edu.tw
[3] Taiwan Semiconductor Manufacturing Company
Hsinchu 300, Taiwan
[4] Yuan Ze University
Jhongli 320, Taiwan
[5] Win Semiconductors Corporation
Taoyuan 333, Taiwan
[6] Industrial Technology Research Institute
Hsinchu 300, Taiwan.

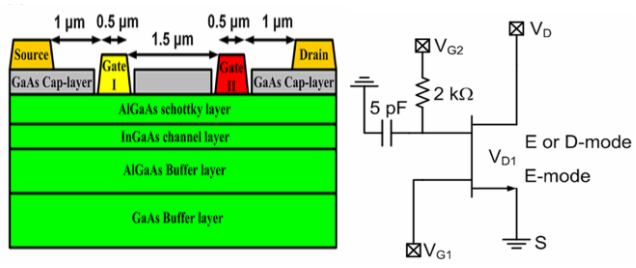
1. Introduction

Low noise amplifiers (LNA) are important to the initial gain stage of wireless receivers. Pseudomorphic high electron mobility transistors (pHEMTs) are always adopted for LNA applications requiring low noise and high gain performance.

Excellent RF (2.4/5.6 GHz) performance has been demonstrated by dual-gate FETs approaching that of cascode structures [1, 2]. This indicates that the cascode topology could be replaced by dual-gate structures to achieve similar noise performance with a reduction in chip size. In this study, we compare the minimum noise figure (NF_{min}), associated gain (G_A), and output power of single-gate D- and E-mode devices, and dual-gate E/E- and E/D-mode devices. The noise results show that the performance of NF_{min} of dual-gate E/E- and E/D-mode devices is similar or superior to that of single-gate devices in the frequency range of 1 to 10 GHz, with improvements in G_A of no less than 8 dB. At 5 GHz, single-gate E-mode device demonstrates the highest noise/power performance.

2. Device Structure and Noise Performance

In the study, single-gate E-, single-gate D-, dual-gate E/E-, and dual-gate E/D-mode pHEMTs were fabricated on the same 6-inch wafer by *WIN* Semiconductors Corporation. Cross-section of the dual-gate device is shown in Fig. 1(a). Gate metals of Pt/Ti/Pt/Au and Ti/Pt/Au were used for E-mode and D-mode gates, respectively. To analyze the characteristics of dual-gate devices, they must be configured in a cascode circuit structure comprising two single-gate devices (gate-I and gate-II FETs) as shown in figure 1(b). Resistors of 2 kΩ and capacitor of 5 pF were selected for the bias network in the gate-II FET.

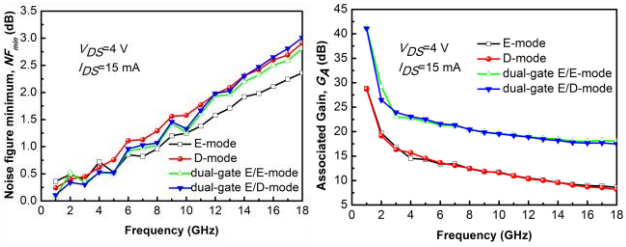


(a) (b)

Fig. 1. Cross-section and equivalent circuit configuration of proposed device. (a) Dual-gate pHEMT, (b) Configuration of cascode circuit for a dual-gate pHEMT with bias network.

Noise performance was characterized at room temperature in a microwave chamber using an ATN noise system. The single-gate E- and D-mode devices were biased at V_{DS} of 4 V and I_{DS} of 15 mA. The dual-gate E/E- and E/D-mode devices were biased under the same conditions with a V_{G2} of 3 V for dual-gate E/E-mode device and 2 V for dual-gate E/D-mode device. The V_{G2} bias was selected to operate both gate-I and gate-II FETs simultaneously in the saturation region (constant current) to obtain maximum gain.

Figure 2 shows the measured NF_{min} and G_A from 1 to 18 GHz for each of the devices. Among the four devices, the single-gate E-mode device demonstrates the lowest NF_{min} between 5 and 18 GHz. The primary reason is the low C_{gs}/g_m ratio in the single-gate E-mode device, as described in (1) from the noise figure analysis of Fukui [3].



(a) (b)

Fig. 2. Measured noise performance of four structures (V_{DS} = 4 V, I_{DS} = 15 mA). (a) Minimum noise figure (NF_{min}), (b) Associated gain (G_A).

$$NF_{\min} = 1 + \frac{2\omega \cdot C_{gs}}{g_m}\sqrt{K_g \cdot g_m \cdot (R_g + R_s)} \quad (1)$$

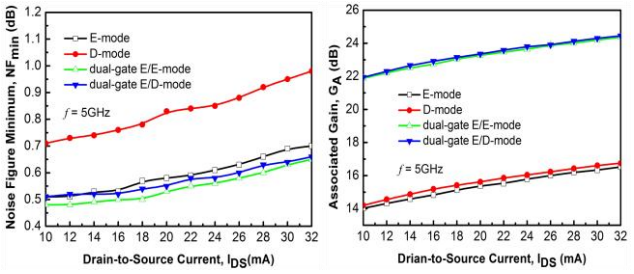
The parameters in (1) can be extracted from a small-signal equivalent-circuit model. Table I lists the values of parameters for four structures extracted at V_{DS} = 4 V and I_{DS} = 15 mA.

Table. I Comparison of small-signal, noise, power characteristics and FOM of single-gate E-mode, D-mode and dual-gate E/E-mode, E/D-mode pHEMTs at V_{DS} = 4 V and I_{DS} = 15 mA. (f = 5 GHz)

pHEMT		E	D	E/E	E/D
Small signal parameters	g_m (mS)	132	82	133	127
	C_{gs} / g_m (f F/mS)	5.89	6.06	6.46	6.91
	R_g (Ω)	1.59	1.39	1.72	1.67
	R_s (Ω)	0.49	0.5	0.3	0.3
Noise parameters	G_A (dB)	14.2	14.5	22.1	22.5
	NF_{min} (dB)	0.53	0.76	0.51	0.52
	R_n (Ω)	7.2	11.8	7.5	7.6
Power characteristics	$P_{in\text{-}1dB}$ & $P_{out\text{-}1dB}$ (dBm)	3 & 16	-3 & 10	-10 & 11	-12 & 8
	IIP3 & OIP3 (dBm)	15.3 & 29.7	12.9 & 26.8	8.9 & 29.0	9.2 & 27.0
FOM [4] (dB/mW)		0.24	0.24	0.37	0.38
FOM [5] (1/mW)		0.66	0.47	1.70	1.76

Since wireless local area networks in 5 GHz frequency band have become popular for portable communication devices. Figures 3(a) and (b) show the measured NF_{min} and G_A under various drain currents (I_{DS}) between 10 mA and 32 mA at 5 GHz.

Figure 4 shows the output power (P_{out}) and intermodulation (IM3) results for the four devices. The dual-gate devices show improvements in power gain as observed in figure 3, but the IM3 (linearity) characteristics are degraded, due to high gain. The noise characteristics shown in figure 3 and power characteristics shown in figure 4 are summarized and compared at 5 GHz in table I.



(a) (b)

Fig. 3. Measured noise performance of four structures at 5 GHz. (a) Minimum noise figure (NF_{min}), (b) Associated gain (G_A).

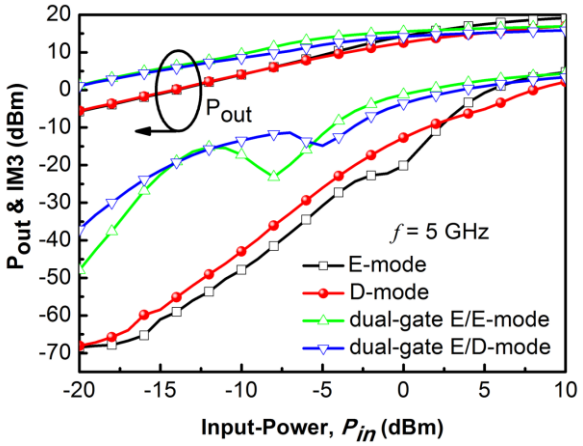


Fig. 4. Measured output power and intermodulation characteristics of the four structures at 5 GHz.

3. Conclusions

The dual-gate E/E- and E/D-mode devices demonstrate excellent low noise and high gain performance in the frequency range of 1 to 10 GHz. These dual-gate devices configured in a cascode circuit structure are equivalent to that of a conventional cascode LNAs comprising two single-gate devices. If power, linearity, and noise are considered simultaneously, single-gate E-mode device presents the highest noise and power performance of the devices in this study at 5 GHz; however, dual-gate E/E- and E/D-mode devices can be biased using a single positive voltage source to simplify complex negative bias networks in integrated LNA circuits.

References

[1] H. Morkner, M. Vice, M. Karakucuk, W. Abey, N. Lan, J. Kessler and R. Ruebusch, "A Single Chip 802.11abgn Enhancement Mode PHEMT MMIC with dual LNAs, Switches, and Distortion Compensation Power Amplifiers," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 365 – 368, June 2007.

[2] M. Nakatsugawa, Y. Yamaguchi and M. Muraguchi, "An L-band ultra-low-power-consumption monolithic low-noise amplifier," *IEEE trans. Microwave Theory Tech.*, Vol. 43, pp. 1745-1750, July, 1995.

[3] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, Vol. 26, pp.1032-1037, Jul. 1979.

[4] Y. S. Wang and Lu L. H., "5.7 GHz low-power variable gain LNA in 0.18 μm CMOS," *Electron Lett.*, Vol. 41, pp. 66-68, Jan. 2005.

[5] I. Song, J. Jeon, H. S. Jhon, J. Kim, B. G. Park, J. D. Lee, and H. Shin, "A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design," *IEEE Electron Device Lett.*, Vol. 29, pp. 1380 – 1382, Dec. 2008.