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Microwave Performance of InGaAs MOSFET with InP Interfacial Layer

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1. Introduction

III-V channel MOSFET is considered as one of the most promising candidates for use in future high speed and RF circuits due to its high electron mobility [1,2]. Recently, several III-V channel NMOSFETs with high-frequency performance have been proposed [3-5]. A record-high f_t of 244 GHz and f_{max} of 292 GHz has been reported for a Lg = 55 nm InGaAs surface channel MOSFET using ALD HfO_2 and Al_2O_3 as gate dielectrics [5]. Buried channel MOSFET have shown higher effective channel mobility compared to surface channel MOSFET [6]. In this paper, the RF characteristics of buried channel InGaAs MOSFETs with InP interfacial layer have been fabricated and studied.

2. Experimental

The schematic diagram of the fabricated buried n-channel InGaAs MOSFET is shown in Fig. 1. The epitaxially wafers grown on semi-insulting InP substrate, Include 300 nm InAlAs grading metamorphic buffer, a 10 nm $In_{0.7}Ga_{0.3}As$ channel layer, a 4 nm InP interfacial layer and a 20 nm N+ $In_{0.53}Ga_{0.47}As$ cap layer.

The process flow of the InGaAs channel nMOSFET is shown in Fig. 2 as following: firstly, InGaAs cap layer, InP interfacial layer and InGaAs channel layer were selectively removed for mesa isolation, then $In_{0.53}Ga_{0.47}As$ cap layer over channel region was removed by using a citric acid based solution. A two-step pre-gate cleaning process was carried out: (1) native oxide removal by using HF, (2) excess elemental arsenic removal by using NH_4OH at room temperature for 5min. 10nm Al_2O_3 was deposited at 300 ^oC as gate dielectric. After that, Ni/Au were e-beam evaporated, followed by a lift-off process to form the gate electrodes. Post metal anneal (PMA) were carried out at 300℃ for 30 sec in a nitrogen ambient. After selectively etching Al_2O_3 by using BOE, S/D electrodes of Ni/Ge/Au/Ge/-Ni/Au were evaporated and patterned by lift-off process, and finally annealed at 270℃ for 3 min.

3. Results and discussion

Fig. 3 shows the output characteristics of a 0.8×25 μm^2 InGaAs MOSFET with a gate bias from -3 to 3 V in steps of 1 V. The drain to gate spacing is 1μm. The maximum drain current is 120 mA/mm at V_{gs} = 3 V and V_{ds} = 2 V. The transfer characteristics or the drain current versus gate voltage of the MOSFET are shown in Fig.3. A maximum extrinsic transconductance (G_{max}) of 60 mS/mm is achieved at V_{gs} = -0.4V and V_{ds} = 2 V.

The effective electron mobility of InGaAs channel has been characterized by using split-CV method. As shown in Fig.3, the fabricated InGaAs nMOSFET exhibited much higher effective electron mobility compared with Si universal mobility. The peak electron mobility of InGaAs channel is 1862 cm^2/eV owing to the InP interfacial layer.

On-wafer S-parameters of a 25 μm gate width InGaAs MOSFET were measured from 100 MHz to 40 GHz, and the device under test was de-embedded using on-chip open and short pad structures. The short circuit current gain (H_{21}) and the Unilateral power gain (U_{max}) were then plotted as a function of frequency. The maximum oscillation frequency ($f$max) was obtained by extrapolation at -20 dB/decade. The typical radio-frequency characteristics of a L_g = 0.8 μm InGaAs MOSFET are shown in Fig.4, f_T of 24.6 GHz and $f$max of 54 GHz have been obtained, respectively.

4. Conclusions

In conclusion, a buried channel InGaAs n-MOSFET with 4 nm InP interfacial layer and 10 nm Al_2O_3 gate oxide was studied. The fabricated InGaAs n-MOSFET exhibited much higher effective electron mobility compared with Si, and the peak electron mobility of InGaAs channel is 1862 cm^2/eV. A 0.8 μm gate length device exhibits a maximum transconductance of 60 mS/mm, a drain current of more than 120 mA/mm, a cutoff frequency (f_T) of 24.6GHz and a maximum oscillation frequency (f_{max}) of 54 GHz, suggesting the viability of these devices for future RF applications.

Acknowledgements

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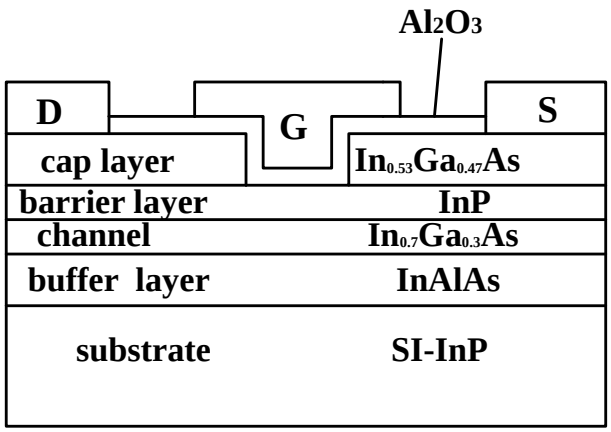

Fig. 1 The cross-sectional schematic diagram of the InGaAs MOSFET with InP interfacial layer.

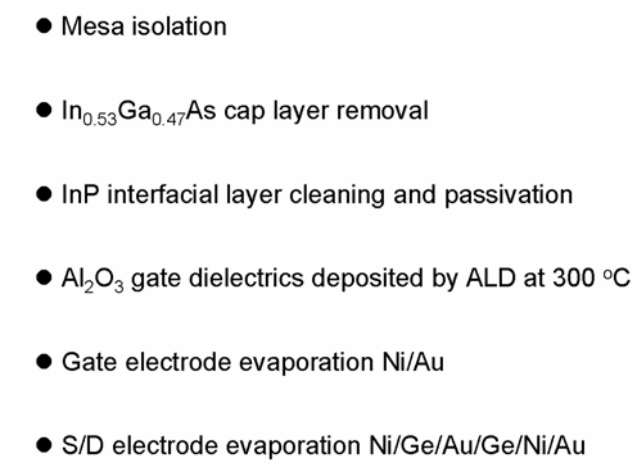

Fig.2 Process flow of the InGaAs MOSFET with InP interfacial layer.

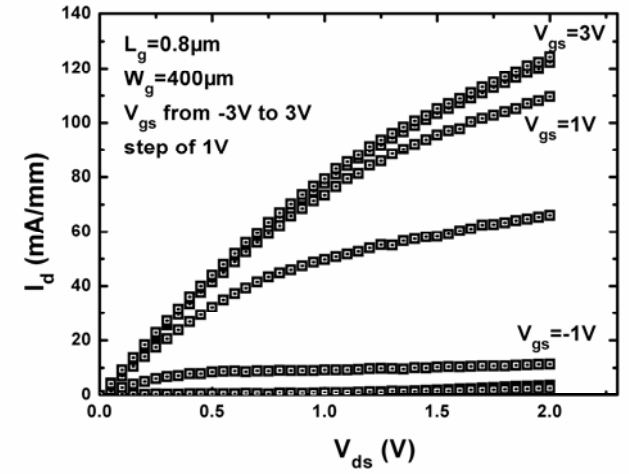

Fig.3. Output characteristics of a L_g= 0.8 μm InGaAs MOSFET

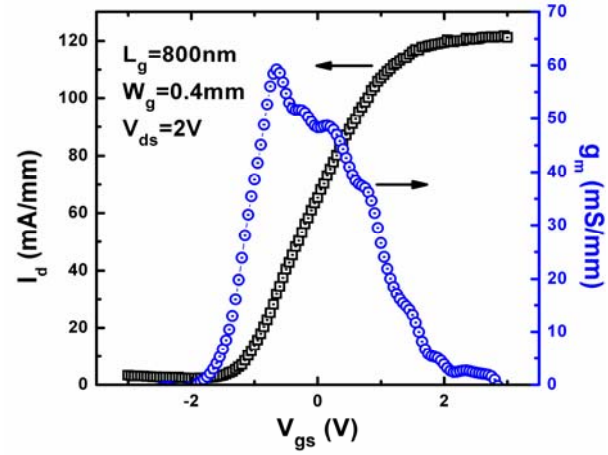

Fig. 4 Transfer characteristics of the InGaAs MOSFET

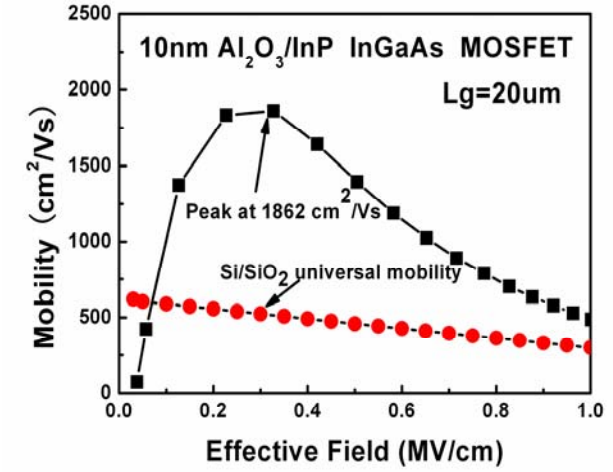

Fig.5 The effective channel mobility versus effective field of InGaAs MOSFET.

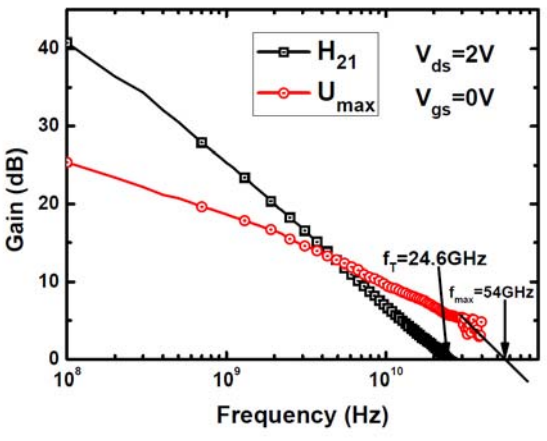

Fig.6 Current gain H_{21} and Unilateral power gain (U_{max}) versus measured frequency for a L_g= 0.8 μm InGaAs MOSFET