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Temperature Effect on Electrical Properties of HfInZnO Amorphous Oxide Thin Film Transistor

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1. Introduction

Amorphous HfInZnO (α-HIZO) is currently considered to be one of the most promising channel materials for the backplane devices of the active-matrix organic light emitting diode (AMOLED). It has genuine characteristics such as transparency, high mobility (> 10 cm^2/V·sec), a possibility of low–temperature process, good uniformity and excellent bias-stress stability [1-3]. Despite these advantages, the instability induced by various stresses such as bias, light, and temperature has still been the critical issues in HIZO TFTs.

Several studies on the instability of HIZO TFT under light and/or dc-bias stress have been recently researched [4-7]. However, the instability caused by only temperature stress excluding light irradiation and dc-bias application has not been reported yet. In most case, the switching TFTs are exposed to various temperatures inevitably, and the unintended change of electric properties occurs by the temperature in consequence. Therefore, temperature-induced instability needs to be newly confirmed.

In this paper, we analyze the instability characteristics at various temperatures ranging from extremely low temperature to high temperature through the fabricated devices. In addition, the mechanism of temperature-induced instability in HIZO TFT is also studied.

2. Experiment

The experimental HIZO oxide semiconductor device had an inverted staggered structure. The gate was formed on a glass wafer with molybdenum. The gate insulators were deposited as a bi-layer consisting of 250-nm thick SiN_x and 50-nm thick SiO_2, where the SiN_x layer was contacted with the gate electrode. Active HIZO with thickness of 40 nm was formed by radio-frequency (RF) sputtering on the gate insulator at room temperature, which consists of In, Zn, O, and Hf [3]. The 100-nm thick protective SiO_2 layer was deposited to prevent the active HIZO from etching damage during source/drain (S/D) wet etching process. Then, the S/D region was sputtered with 200-nm thick molybdenum on the active. For a passivation, the SiO_2 film of 200-nm thickness was grown. Finally, the devices were annealed in the N_2 ambient for 5 h at 250 ℃. All the patterning was simply performed by photolithography and wet/dry etching.

Fig. 1(a) shows the cross sectional TEM image of a finished TFT along the gate length direction. Also, from Fig. 1(b) and (c), it is observed that the fabricated devices are fairly functioned as a transistor.

All the fabricated HIZO TFTs were characterized using the HP4156 precision semiconductor parameter analyzer at various temperatures. Fig. 2(a) shows the transfer characteristics of the fabricated TFTs at various temperatures (273 K, 293 K, 310 K, and 333 K), respectively. The transfer characteristics were measured at the 0.5 V drain bias in the dark.

3. Results and Discussion

There were a threshold voltage (V_{th}) shift in the left direction, subthreshold swing value (*S.S*) degradation, and on-current enhancement as temperature get higher. Also, Fig. 2(b) illustrates the dependence of temperature on V_{th}, *S.S*, and on-current. As compared to Si-based transistors, it should be noted that the on-current increases gradually with higher temperatures due to different conductance mechanism.

In order to investigate the cause of the temperature-induced effects, the current flowing from the source toward the drain (S/D current) was measured with floated gate and grounded source by sweeping a drain voltage at various temperatures (273 K, 293 K, 310 K, and 333 K). In result, Fig. 3 indicates that the exponential increase of the S/D current occurs as temperature gets higher. This phenomenon can be explained as follows. Based on Fig. 3, it is expected that the metal contacted with the channel in source/drain regions forms a Schottky barrier diode (SBD) rather than an ohmic contact with small resistance [8]. Thus, HIZO TFTs can be modeled as two oppositely connected SBDs which are modulated by a gate bias [9-11]. Here, The S/D current passing through the channel is dominantly supplied by the source-sided SBD, and consists of thermionic emission and field-induced tunneling components like a Schottky barrier FET. Consequently, the thermionic emission component increases significantly with higher temperatures. This causes the V_{th} shift, *S.S* degradation, and on-current enhancement.

As above-mentioned, we have observed that the thermionic emission enhanced by temperature results in the V_{th} shift, S.S degradation, and on-current enhancement in terms of transfer curves. However, unfortunately, the electric properties vary slightly with temperature increase. Furthermore, transfer curves can be measured within the limited range of temperature since the intrinsic properties of α-HIZO film would be changed at over limited high temperature. Therefore, the transfer characteristics were

confirmed at extremely low temperature (100 K) instead of exceedingly high temperature.

As the result, Fig. 4(a) presents that a V_{th} shift in the right direction and on-current reduction occurs significantly at the same time. This implies that the thermionic emission is dramatically reduced, while the field-induced tunneling remains nearly unchanged. This phenomenon can also be verified from the S/D current extracted at extremely low temperature (100 K). As shown in Fig. 4(b), the S/D current has the significant reduction with temperature lowering in a linear scale. Moreover, the inset of Fig. 4(b) illustrates that the S/D current keeps noise level as low as 10^{-11} A with negligible thermionic emission component, and the S/D current increases abruptly at critical drain voltage (V_{DS} = about 4 V) on a logarithmic scale since field-induced tunneling starts to occur at the critical voltage.

Based on Figs. 4(a) and (b), it is clearly concluded that the only thermionic emission component out of total S/D current is suppressed whereas field-induced tunneling component is hardly affected by low temperature, resulting in the evident V_{th} shift in right direction and on-current reduction.

4. Conclusion

In summary, temperature-induced effect on the electric properties in α-HIZO TFT was investigated rigorously. The S/D current measurements were carried out through systematic approaches to clarify the underlying physical cause. As the result, it is clearly found that the S/D metal contacted with the HIZO channel forms a Schottky barrier diode, leading to the temperature-induced change of the electric properties.

References

[1] J.-H. Lee, *et al.*, *IEEE Elec. Dev. Lett.*, **27**(2006) 830.
[2] C. Goncalves, *et al.*, *Thin Solid Film*, **516**(2008) 1374.
[3] C.-J. Kim, *et al.*, *Appl. Phys. Lett.*, **95**(2009) 252103.
[4] E. Chong, *et al.*, *Appl. Phys. Lett.*, **96**(2010) 152102.
[5] J. S. Park, *et al.*, *Appl. Phys. Lett.*, **96**(2010) 262109.
[6] J. S. Park, *et al.*, *IEEE Elec. Dev. Lett.*, **31**(2010) 440.
[7] J. H. Shin, *et al.*, *ETRI Journal*, **31**(2009) 62.
[8] I. H. Song, *et al.*, *IEEE Elec. Dev. Lett.,* **29**(2008) 549.
[9] J. M. Larson, *et al.*, *IEEE Trans. Elec. Dev.,* **53**(2006) 1048.
[10] S. Zhu, *et al.*, *IEEE Elec. Dev. Lett.,* **25**(2004) 268.
[11] S. Zhu, *et al.*, *IEEE Elec. Dev. Lett.,* **25**(2004) 565.

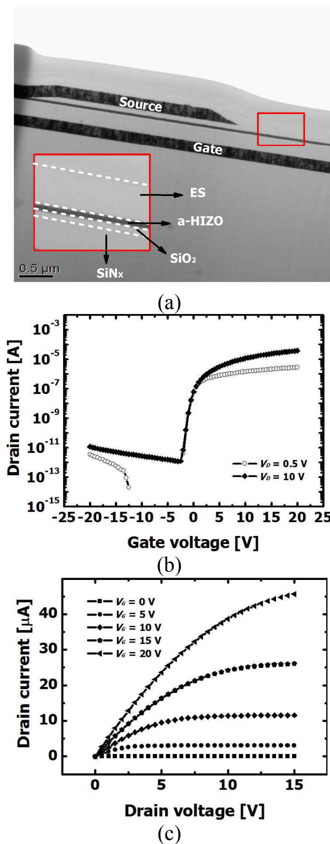

Fig. 1. (a) Cross- sectional TEM image of the fabricated HIZO TFT along the gate length direction. (b) Transfer characteristics of HIZO TFTs with various drain voltages. The on-to-off ratio is nearly 10^6. The off-current is low as less than 10-[11] A, and the on-current is higher than 10^5 A for V_{DS} = 10 V. (c) Output characteristics of HIZO TFTs with various gate voltages.

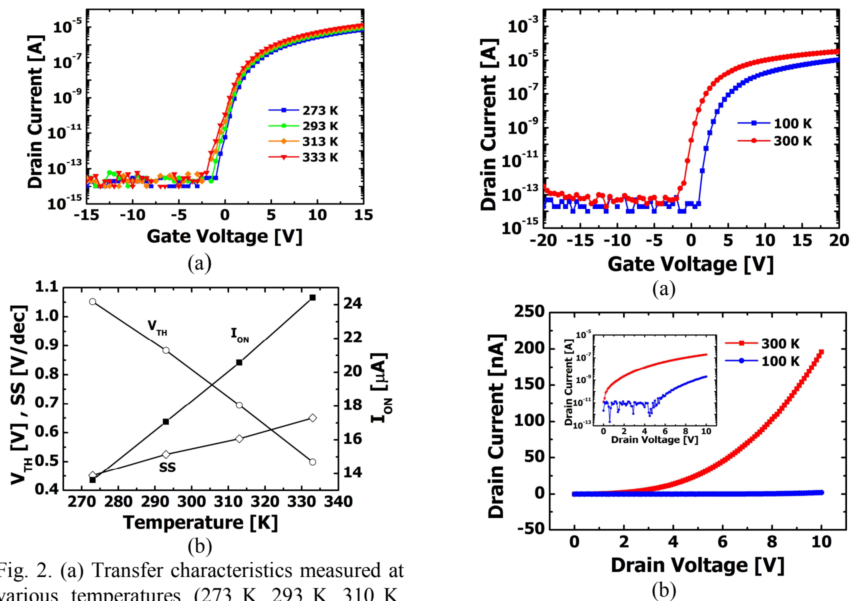

Fig. 2. (a) Transfer characteristics measured at various temperatures (273 K, 293 K, 310 K, and 333 K). (b) Dependence of temperature on the threshold voltage (V_{th}), subthreshold swing value (S.S), and on-current (I_{on}).

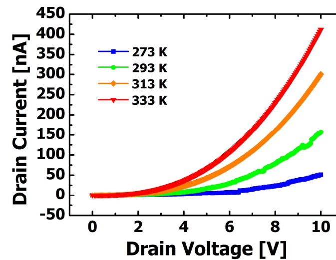

Fig. 3. Current-voltage characteristics of HIZO TFTs between source and drain under floated gate and grounded source by sweeping a drain voltage.

Fig. 4. (a) Transfer characteristics measured at extremely low temperature (100 K). (b) Current-voltage characteristics between source and drain at extremely low temperature in a linear scale (the inset also shows the current-voltage characteristics on a logarithmic scale).