Extended Abstracts of the 2012 International Conference on Solid State Devices and Materials, Kyoto, 2012, pp190-191

High Performance Dual-layer Channel ZnO Thin-Film Transistor

Youfeng Geng[2,1], Dedong Han[1*], Jian Cai[1], Wei Wang[1], Liangliang Wang[1], Yu Tian[1], Huikun Yao[1], Lixun Qian[3], Yi Wang[1] and Shengdong Zhang[2*]

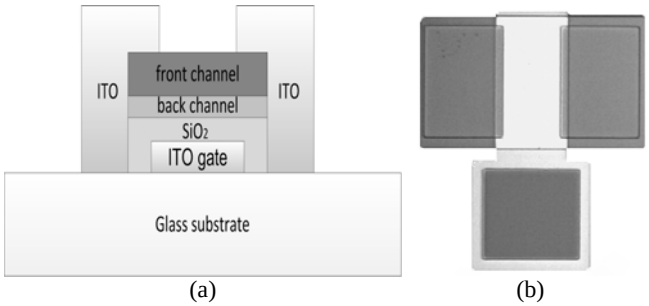
[1]Institute of Microelectronics, Peking University, Beijing 100871, PRC
[2]Shenzhen Graduate School, Peking University, Shenzhen 518055, PRC
[3]Beijing Institute of Technology, Beijing 100081, PRC
Phone: +86-10-62753144 Fax : +86-10-62751789 *E-mail: zhangsd@pku.edu.cn, handedong@pku.edu.cn

1. Introduction

Thin film transistor (TFT) based on ZnO material has attracted much attention for its potential properties[1]. The field effect mobility of ZnO TFT reported in the literature is high even fabricated at low temperature[2]. Moreover, ZnO has a wide bandgap (~3.3eV) which leads to a good transparence in visible region of the spectrum[3]. Nevertheless ZnO thin film tends to form polycrystalline structure during deposition. The random grain size of polycrystalline ZnO can cause serious nonuniformity from transistor to transistor, which is a fatal weakness for its application[4]. In this paper, our research group utilizes the dual-layer channel structure to reduce the nonuniformity and improve the performance. A thin and low O_2/Ar ratio ZnO layer provides a well conductive and amorphous channel, whereas a thick and high O_2/Ar ratio ZnO layer limits the off-state currents. The effects of annealing are also analyzed by comparing the characteristics of devices before and after annealing.

2. Device Fabrication

The cross sectional schematic of the inverted staggered dual-layer channel ZnO TFT is shown in Figure 1(a). Firstly, Indium Tin Oxide (ITO) (130nm) was deposited on glass substrate by radio frequency (RF) sputtering, and patterned by lift-off technology. Next, SiO_2(150nm) was deposited by plasma enhanced chemical vapor deposition (PECVD). Subsequently, dual-layer ZnO active region was deposited by RF sputtering with low and high O_2/Ar ratio respectively. Then SiO_2 layer and ZnO layer were patterned by lift-off technology at the same time. Finally, an ITO layer (130nm) was deposited by RF sputtering to form source and drain electrodes. The optical micrograph of the ZnO TFT is shown in Figure 1(b).



(a) (b)

Fig.1 (a) Schematic cross section of the dual-layer channel ZnO TFT (b) Optical micrograph of a fabricated ZnO TFT.

Current-voltage curves of the ZnO TFT were measured using a semiconductor analyzer (Agilent 4156C) at room temperature.

3. Analysis and Discussion

To investigate the influence of O_2/Ar ratio to the dual-layer channel ZnO TFT, the configuration of different conditions was set as shown in Table I.

Table I Configuration of different conditions

device	back channel		front channel	
	O_2/Ar ratio	thickness	O_2/Ar ratio	thickness
A	0/100(sccm)	15(nm)	10/90(sccm)	60(nm)
B	2/98(sccm)	15(nm)	10/90(sccm)	60(nm)

Shown in the Figure 2 are the XRD spectra of ZnO thin film deposited on the glass substrate with different thickness and O_2/Ar ratios. The spectra show that the ZnO thin film is amorphous when the thickness of the film is around 15nm, and it is polycrystalline when the thickness is around 60nm. This result indicates that the ZnO thin film tends to form amorphous structure when the ZnO film is very thin[5]. Even after annealing at 280℃, the thin ZnO film still remained amorphous as shown in Figure 2. When the TFTs turn on, the currents just crowd in a thin layer of channel[6]. As the back channel is amorphous, dual-layer channel structure can reduce the nonuniformity caused by the polycrystalline structure of ZnO thin film.

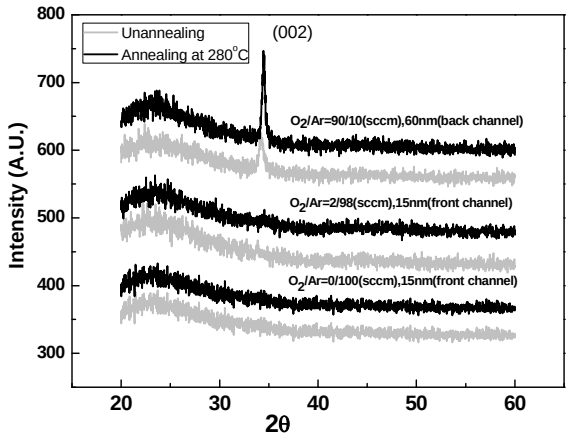


Fig. 2 XRD Spectra of ZnO thin film deposited on glass substrate at different conditions before and after annealing.

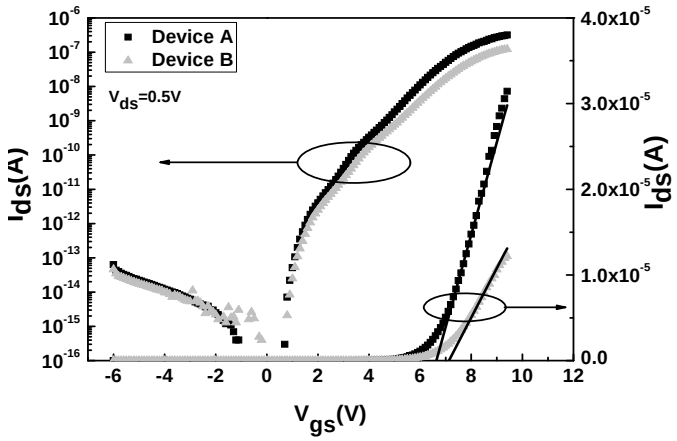


Fig. 3 The transfer characteristics of ZnO TFT without annealing

The transfer characteristics of ZnO TFT without annealing are shown in Figure 3. Device A has typical values of V_{th}=6.6V, μ =66.4cm^2/Vs, $I_{on}/I_{off}=10^8$, S=0.75V/decade, and device B exhibits a performance of V_{th}=7.2V, μ =35.8cm^2/Vs, $I_{on}/I_{off}=10^7$, S=1.09V/decade. The results indicate a high mobility than the most recent reports on ZnO TFT. The high mobility may origin from the dual-layer channel structure. As the back channel sputtered at low O_2/Ar ratio, it contained a large amount of oxygen vacancies. With the gate voltage increasing, electrons accumulate gradually in the interface of insulator and active layer leaving quantity of fixed positive charges in a thin layer. These fixed positive charges can attract the electrons off the interface and form a buried channel, as shown in Figure 4. The number of defects existing in the buried channel is smaller than that in the interface of insulator and active layer. Thus the mobility of carrier can be high.

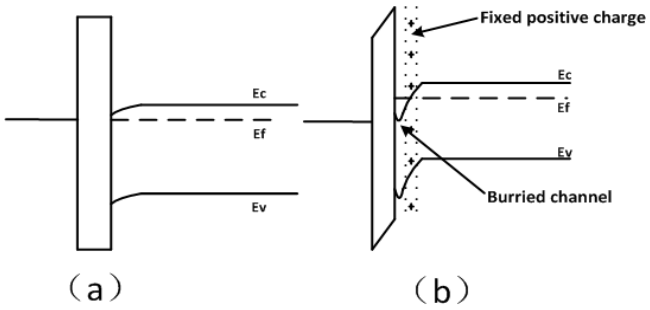


Fig. 4 The schematic band diagram of dual-layer channel ZnO TFT, (a) equilibrium, (b) on positive bias.

Typical transfer and output characteristics of device A and B annealing in the air ambience at 280℃ are shown in Figure 5. For the transfer characteristic of device A at V_{ds}=0.1V, a V_{th} of 5.2V, a μ_{EF} of ~129cm^2/Vs, an I_{on}/I_{off} of 10^6, an S of 0.66V/decade are extracted. For device B, it has a V_{th} of 5.5V, a μ_{EF} of 13cm^2/Vs, an I_{on}/I_{off} of 10^6, and an S of 0.83V/decade. The mobility of device A increases, but it declines for device B after annealing. As discussed above, the back channel of device B was deposited at high O_2/Ar ratio, so the number of oxygen vacancy is less than that of device A. Therefore after annealing in the air, device A still had enough fixed positive charges to attract the currents off the interface of insulator and active layer to form buried channel but device B didn't. This result confirmed that dual layer channel can improve the mobility of ZnO TFT obviously through forming buried channel. The output characteristics of device B in the insert picture of Figure 5 are well-behaved, showing obvious saturation at sufficiently high V_{ds}.

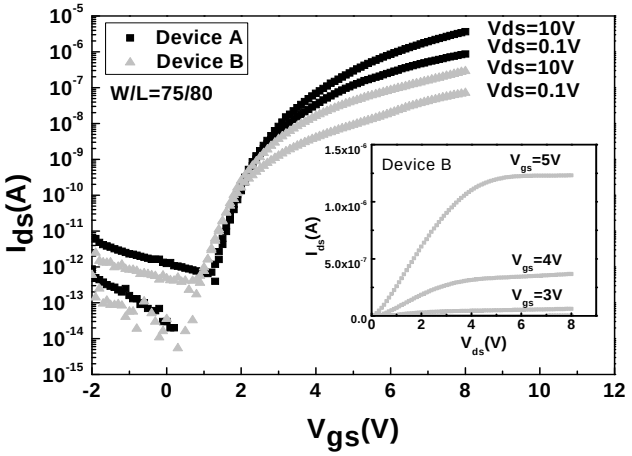


Fig. 5 The I-V characteristics of dual-layer channel ZnO TFT after annealing

4. Conclusions

In conclusion, we demonstrated a dual-layer channel ZnO TFT with the best performance of a threshold voltage of 5.2V, a mobility of 129cm^2/Vs, an I_{on}/I_{off} ratio of 10^6, a sub threshold voltage of 0.66V/decade after annealing. The dual-layer channel structure can improve mobility obviously, and the origin of high carrier mobility was explored.

Acknowledgments

This work is supported by the National Natural Sci ence Foundation of China (Grant No. 60976041 and 6 0977016) and by the National Basic Research Program of China (973 program, Grant No. 2011CBA00600).

References

[1] U. Ozgur, *Proceedings of the IEEE*, (2010) 98, 1255.

[2] U. Ozgur, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan; V. Avrutin; S. J. Cho, H. Morkoc, J. Appl Phys, (2005) 98, 041301.

[3] L. Chien Cheng, W. Meng Lun, L. Kuang Chung, H. Shih-Hua, C. Yu Sheng, L. Gong-Ru, H. JianJang, Display Technology, Journal of, (2009) 5, 192.

[4] H. Bong, W. H. Lee, D. Y. Lee, B. J. Kim, J. H. Cho, K. Cho, Appl Phys Lett, (2010) 96, 192115.

[5] H. H. Hsieh and CC. Wu, Appl Phys Lett, (2007) 91, 013502.

[6] F. Torricelli, J. R. Meijboom, E. Smits, A. K. Tripathi, M. Ferroni, S. Federici , Electron Devices, IEEE Transactions on, (2011) 58, 2610.