Fabrication of Backside-Illuminated CMOS Compatible Photodiode for Optoelectronic Integrated Circuits

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1. Introduction

The optical interconnection interface between light source and control circuit, need for realizing of monolithic optoelectronic integrated circuits (OEICs) [1-4]. And development and structural design of the optical receiving element also needs. Photodiode is the semiconductor device which generates optical current by the absorption of light as a detector [5, 6]. It can be used in optical communication systems because of excellent features which of linear output, wide spectral response and most of all compatibility of complementary metal oxide semiconductor (CMOS) process. Few years ago, Sony Corporation presented the backside-illuminated (BSI) sensor for using a novel arrangement of the imaging elements to increase the amount of light captured and thereby improve low-light performance. This BSI sensor has the essential features to achieve high image resolutions with small modules sizes using silicon on wafer (SOI) substrate [7]. Generally BSI sensors were produced by on the SOI wafer after formation the circuitry and removing the BOX carrier. This fabrication process needs very complex treatment and high cost with the special equipments. Micro-electro mechanical system (MEMS) processing is promising technology that enables for applying mass production of ultra-small semiconductor micromanipulation processing and lower power consumption in next generation microelectronics. On the whole, to make the integrated structure of the MEMS elements and circuit, silicon substrate is etched by dry method using a mask of oxide films which of deposited by plasma enhancement chemical vapor deposition (PECVD), or photo-resist. However, PECVD oxide layer cannot be used for deep reactive ion etching (RIE) etching mask (over 100 µm of etching) because of the unstable chemical stoichiometry and low density. Normally, wet oxidation method of the oxide film is formed at both sides of wafer by the thermal furnace according to the process time at 0.6 $um \sim$ 1.2um thickness.



Fig. 1 Conceptive Scheme of This Work

Local oxidation of silicon (LOCOS) process is method of standard CMOS process for electrically isolation of each component. By using this oxide layer, deep RIE can be used as high resist etching mask for MEMS devices. Our research group has been study of heterogeneous OEICs from the past few years [8, 9]. The heterogeneous integration technology is one of the concept of overcome the process limits by the fundamental problems as a lattice mismatch. To using this, the devices can be monolithically integrated without re-growth by bonding process. Figure 1 shows conceptive image of this work which of heterogeneous OEICs with BSI photodiodes. In this study, firstly, we proposed fabrication process with practical formation method of the BSI photodiode by using MEMS and post-CMOS process. Then, fabricated BSI photodiode was used as an optical receiver with trans-impedance operational amplifier (OPAMP) and pulse width modulator (PWM) as a prototype optical interconnection system.

2. Experiment and Results

Design and fabrication of BSI photodiode

Figure 2 shows the designed mask layout and cross-sectional structure of BSI photodiode. Fabrication of this BSI photodiode in the CMOS process has advantage that needs only one additional process. In the polished p-type wafer (thickness of 350 μ m), light doped n-well was formed by as CMOS n-well ion-implantation and drive in process. For light receive region, back-side SiN₄ layer was patterned by using both-side aligner. The field oxide (FOX) and oxidation layer of back side for deep RIE process were grown by LOCOS process. n+ and p+ are formed by n, p-MOS source / drain ion-implantation process. To block the light from the surface, the whole surface of n-well region and the part of FOX were covered by aluminum metal pad. The back side illuminated pattern (deep-RIE) was des-



Fig. 2 Mask Layout Design and Cross-Sectional Structure of BSI Photodiode (Dimensions of cross-sectional image were not scaled)



Fig. 3 Output Current density versus Input Voltage Characteristics of Fabricated BSI Photodiode

igned 5 μ m larger of four sides than sensing area size. The deep RIE process was performed using SF₆ and C₄F₈ gas as various cycle times. For etching backside wafer about thickness of 340 μ m, DRIE was performed of 420 cycles for 2 hours 30 minutes after photo-resist coating. *Results*

Figure 3 shows I-V curves of photodiode which of the light receive area size of $80 \times 80 \ \mu m^2$ with incident light power of 1.86×10^3 Watt / m² and wavelength of 670 nm. Quantum efficiency and responsivity were obtained of 28.4% and 0.163, respectively under reverse bias voltage of -2V. Dark current was measured approximately 800 fA under same reverse bias voltage. Figure 4 shows the circuit diagram of optical current amplifier as trans-impedance OPAMP. The resistor R_F (9.7 M Ω) was introduced for adjusting of amplifiable voltage from optical current of the photodiode. The capacitor C is the role of a filter to remove noise from power supply. Figure 5 shows the results of amplified and modulated signal by integrated circuits as various optical input powers. The optical current of BSI photodiode was amplified to voltage of the range of 0.54 V to V_{DD} (5V) The reason of minimum voltage of 0.54 V was caused by external capacitor due to filtering noise from sawtooth wave generator. The compared signals, which of sawtooth and amplified signal, were generated the inverted



Fig. 4 Circuit Diagram of Optical Current to PWM Wave Modulator



Fig. 5 Results of Modulated Optical Current as Various Duty Ratios According of Light Intensity

PWM waves. The duty ratio control was possible up to 83.6%. This result is attributed to minimum output voltage range of the optical current amplifier.

3. Conclusions

The prototype OEICs devices with operating by optical interconnections were proposed and fabricated. Firstly, the features of BSI photodiode were introduced. Then, for implement of device, BSI photodiode was designed and demonstrated as CMOS compatible practical method by utilizing MEMS and post-CMOS process. The optical current of fabricated BSI photodiode was converted to pulse width modulated signal for implementing of the optical interconnection.

Acknowledgements

This study was supported in part by the Regional Innovation Cluster Program from the MEXT, Japan. Device processes were carried out at Electronic Inspired Interdisciplinary Research Institute, Toyohashi Tech.

References

[1] J. W. Goodman, F. J. Leonberger, S. Y Kung and R. A. Athale, Proc. IEEE **72** (1984) 850.

- [2] H. K. Choi, G. W. Turner, T. H. Windhorn and B. Tsaur, IEEE Electron Device Lett. **EDL-7** (1986) 500.
- [3] I. Hayashi, Jpn. J. Appl. Phys. 32 (1993) 266.
- [4] H. Yonezu, Semicond. Sci. Technol. 17 (2002) 762.
- [5] S. Han and E. Yoon, Ele. Lett. 42 (2006) 20.
- [6] I. Brouk, K. Alameh and Y. Nemirovsky, IEEE Tran. Elec. 54 (2007) 468.
- [7] J. Prima, F. Roy, P. Coudrain, X. Gagnard, J. Segura, Y. Cazaux, D. Herault, N. Virollet, N. Moussy, B. Giffard, P. Gidon, *Proc. Int. Image Sensor Workshop* (2007) 5.

[8] S. B. Shin, K. Iijima, J. Chiba, H. Okada, S. Iwayama and A. Wakahara, Jpn. J. Appl. Phys. 32 (2011) 04DG12.

[9] S. B. Shin, K. Iijima, H. Okada, S. Iwayama and A. Wakahara, IEICE Trans. ELEC. E95-C (2012) 898.