

Silicon-based Floating-body Synaptic Transistor

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1. Introduction

Recently there have been very interesting attempts to mimic the memory operation of the biological system with microelectronics technology in pursuit of alternative architectures for ultralow power solid-state system [1-3]. However, most of these electronic synaptic systems ended up in showing either short-term plasticity (STP) or long-term potentiation (LTP), while biological systems use both mechanisms to make the memorization process more efficient as shown in Fig. 1 [4, 5]. Here we propose a novel Si-based device structure, so called Si-based Floating-body Synaptic Transistor (SFST), to emulate both STP and LTP characteristics with a single device. Floating-body effect and hot hole injection are used to store synaptic weight as short-term and long-term memories respectively. The learning mechanism of the device is demonstrated with a commercial ATLASTM TCAD device simulator.

2. Results and Discussion

2.1 Device Configuration

The structure of SFST is described in Fig. 2 and Table I. It is based on the capacitor-less DRAM except the backside part. By locating the floating gate at backside, we intend SFST to have LTP characteristics. The transition from STP to LTP occurs automatically. In addition, it is meaningful that SFST can be fabricated using existing Si-technology because it is composed of only silicon and silicon oxide.

2.2 Learning Mechanism

First of all, the transient characteristic is investigated with constant input signals ($V_g = V_d = 1$ V, $V_s = 0$ V, $V_{cg} = -6$ V) assuming the interval of input pulses (T_i) as 0 s. When right after input signals are applied, the excess holes are generated by impact ionization near the surface because the negative V_{cg} makes potential barrier between source and body (Fig. 3). These excess holes are pulled to bottom of silicon and the accumulation of holes results in short-term reinforcement of synaptic weight, which is STP. This behavior is similar to the capacitor-less DRAM.

Moreover, impact ionization much occurs because the excess holes lower potential barrier by the negative V_{cg} . This results in positive feedback increasing the excess hole generation rate because more electrons come over potential barrier (Fig. 4). Fig. 5 shows that body hole concentration, which is the integration of hole concentration over cross section of silicon body, increases exponentially over time before the triggering point.

Through positive feedback loop described above, the source-body junction at bottom of silicon becomes forward

biased at a certain point and then a lot of electrons go over body from source (Fig. 6). This is similar to triggering operation of the thyristor. As a result, impact ionization and body hole concentration increase dramatically (Fig. 5) and hot hole injection into floating gate occurs (Fig. 7) to result in LTP. Note that the transition from short-term memory to long-term memory is achieved without any change of bias condition.

Fig. 8 shows transient characteristic of synaptic weight with time of input signals. The synaptic weight is estimated as drain current at a read condition ($V_g = 0.3$ V, $V_d = 0.1$ V, $V_s = V_{cg} = 0$ V). For STP, the temporary enhanced synaptic weight is decreased to initial low level current due to the recombination of the excess holes, which is the forgetting process. On the other hand, in case of LTP, the synaptic weight remains at a high current level constantly with the nonvolatile memory property. Fig. 9 shows that most of electrons flow through the bottom of silicon at LTP due to positive charges in the floating gate.

2.3 Response to Input Pulse Train

Response of SFST with T_i is also investigated. Input pulses with a width of 0.1 μ s are applied 10 times at intervals of 10 μ s and 100 μ s. With a lower repetition rate ($T_i = 100$ μ s), body hole concentration decreases during intervals between pulse (Fig. 10). The amount of recombination of the excess hole increases as body hole concentration increases. Therefore, there is no triggering operation in spite of 1 μ s total input time. With a faster repetition rate ($T_i = 10$ μ s), however, Q_{FG} starts increasing from the seventh input, which means that the switch from STP to LTP is made by hot hole injection (Fig. 11). These are obvious evidences of time-dependent synaptic behavior.

3. Conclusions

A novel Si-based Floating-body Synaptic Transistor (SFST) was proposed. The synaptic learning mechanism of SFST was explained. The triggering action from STP to LTP could be obtained by positive feedback between the excess holes and impact ionization without any application of bias voltage. Frequency response of SFST was also demonstrated. The synaptic weight of SFST was dependent on the input pulse interval in spite of same total input time.

Acknowledgements

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References

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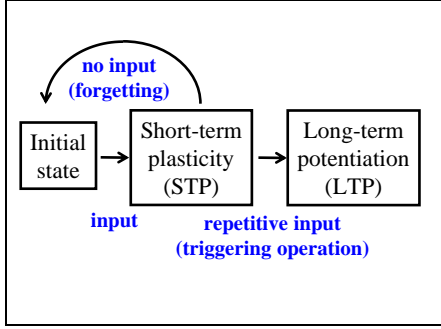


Fig. 1 Processing flow of Hebbian learning with STP and LTP.

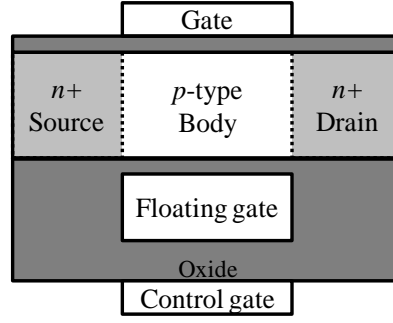


Fig. 2 Structure of the proposed SFST.

Table I Parameters used in the simulation.

Parameters	Value
Body thickness	10 nm
Channel length	100 nm
Body doping concentration	10^{18} cm^{-3}
S/D doping concentration	10^{21} cm^{-3}
Gate oxide thickness	3 nm
Blocking oxide thickness	8 nm

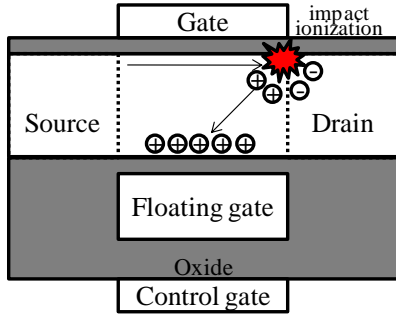


Fig. 3 Schematic view of STP formation mechanism.

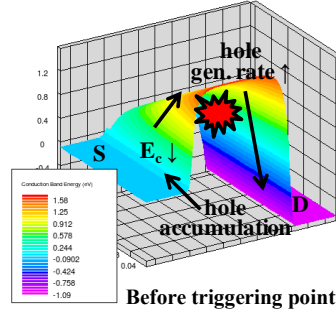


Fig. 4 3D energy band contour of conduction band and positive feedback scheme.

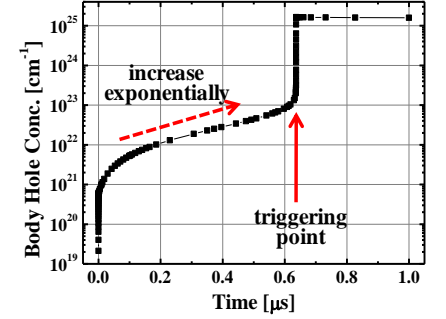


Fig. 5 Transient characteristics of body hole concentration.

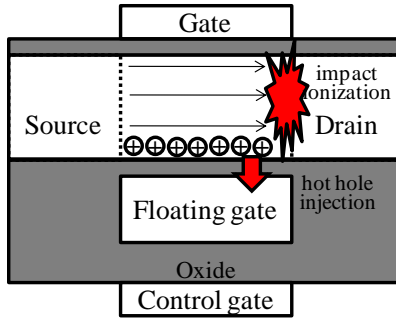


Fig. 6 Schematic view of LTP formation mechanism.

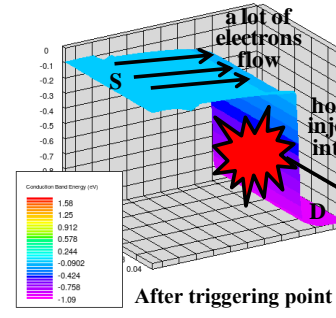


Fig. 7 3D energy band contour of conduction band and flow of electrons.

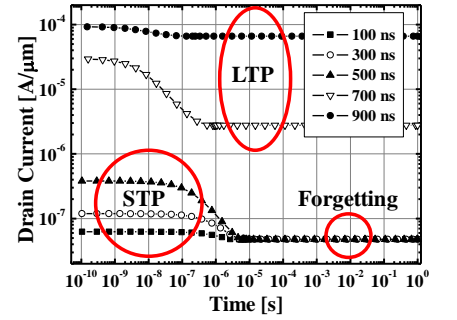


Fig. 8 Read current (synaptic weight) of SFST with time of input signals.

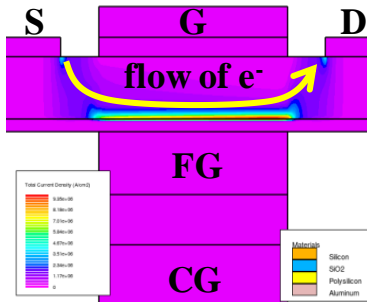


Fig. 9 Contour of electrons current density at LTP read condition.

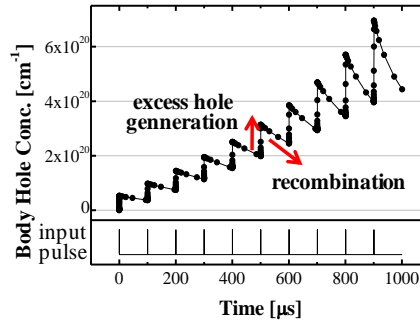


Fig. 10 Change in the body hole concentration when $T_i = 100 \mu\text{s}$.

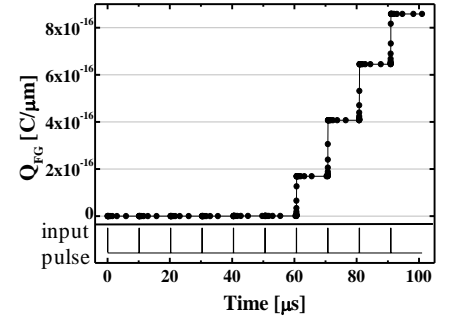


Fig. 11 Change in Q_{FG} when $T_i = 10 \mu\text{s}$.