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Resistance switching memory characteristics of $Si/CaF_2/CdF_2$ quantum-well structures grown on metal($CoSi_2$) layer

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1. Introduction

The dimension of the elements consisting integrated circuits is going down into nano-scale. One essential building block for nanoscale solid state devices is electric potential sequences for controlling electron transport, which can be implemented using energy band discontinuity at atomically abrupt heterointerfaces. A $CdF_2/CaF_2/Si$ heterostructure is an attractive candidate for applications on Si substrates, such as resonant tunneling diodes (RTDs) [1] and transisters [2] coulomb blockade devices, because of the large conduction band discontinuity (ΔE_C~2.9eV) at the heterointerface [3] and small lattice mismatch with silicon. Due to the large ΔE_C, leakage current is expected to be suppressed in low level even at room temperature and moreover, voltage for tunneling transport can be controlled by utilizing multi-quantum-well tunneling scheme such as resonant tunneling or sequential tunneling with appropriate design of quantum-well layer thickness sequences. Up to now, we have demonstrated large ON/OFF current ratio of CdF_2/CaF_2 RTDs larger than 10^5 at RT [4-6], which confirmed advantage of the large ΔE_C heterostructure material systems. And moreover, we have proposed and demonstrated novel scheme of resistance switching diode or resistance random access memory (ReRAM) cell using $Si/CaF_2/CdF_2/CaF_2/Si$ quantum-well (QW) structure [7, 8]. For high-integration of ReRAM cell, we have proposed cross point array scheme using silicide based metallic lead line arrays expecting low resistivity and high-quality heterointerfaces because of similar crystal structure and small lattice mismatch with Si and fluorides.

In this study, we have investigated formation technique of the $Si/CaF_2/CdF_2/CaF_2/Si$ QW structures on $CoSi_2$ layers formed by using solid phase epitaxy with protective oxide layer for surfactant. Resistance switching at room temperature has been clearly observed. And moreover, stability and reproducibility of I-V characteristics has been significantly improved. Using the technique, fabrication of memory cell array on $CoSi_2$ lead line has been successfully demonstrated.

2. Structure and operation principle

Figure 1 shows schematic device structure and band diagram (flat band) used in this study. Basic concept of the device is $CaF_2/CdF_2/CaF_2$ double-barrier resonant tunneling diode structure or quantum-well (QW) structure sandwiched by silicon as the secondary energy barriers. CaF_2 layers act as energy barriers mainly for charge injection and ejection between a CdF_2 QW and a reservoir of electrons. Si layers act as energy barriers for suppression of electron escape from the CdF_2 QW. Using this layer configuration, write/erase voltage can be controlled by designing the appropriate thickness of CdF_2 quantum-well (2.5 nm-thick CdF_2 QW provides 1 V switching voltage for example) based on resonant tunneling scheme. Injected electrons are retained in CdF_2 QW because conduction band minimum of CdF_2 is ~0.6eV lower than that of Si therefore retention time can be controlled by the thickness of n-Si barrier layer. In writing operation, electrons are injected from a metal (Al) layer or n-type Si layer by resonant tunneling or sequential tunneling and a part of the electrons are trapped in CdF_2 QW. Trapped electrons are steeply increased at around peak voltage (V_{peak}) because electron injection rapidly increases at around V_{peak}. Therefore, resistance switching occurs at around V_{peak} of a $CaF_2/CdF_2/CaF_2$ RTD. Resistance modulation (ON/OFF) ratio of more than 1000 can be expected theoretically due to the difference of tunneling probability between charged states and uncharged states of CdF_2-QW. And moreover, retention time should be strongly affected by the thickness of n-Si barrier layer. For the future high-integration of resistance switching memory cell, fabrication technique of the cell on the low resistance metallic lead line is strongly required. In this study, $CoSi_2$ was used for the metallic lead line because of the availability of epitaxial growth technique of fluorides/silicon heterostructures on $CoSi_2$ and potential compatibility of LSI processes.

3. Experiment

An 80 nm-thick SiO_2 layer was formed on a p-type Si(111) 0.1° off substrate with resistivity of less than 4 mΩ·cm using thermal oxidation at 900°C. Subsequently, 2 μm-diameter holes were formed by BHF etching for sample B, which provides hydrogen-terminated Si surface. On the other hand, protective wet oxide layers on Si surface at the bottom of the holes was formed by SPM for sample A. After loaded into the ultra-high-vacuum (UHV) chamber, 10-nm-thick Co was deposited at RT followed by in-situ annealing at 550°C for 30 min, which yields $CoSi_2$ layer with resistivity of ρ ~ 13 μΩ·cm for both cases as schematically shown in Fig.2. Subsequently, $Si/CaF_2/CdF_2/CaF_2/Si$ multilayered heterostructures were grown on the $CoSi_2$ using molecular beam epitaxy (MBE) based technique. Residual protective oxide as a surfactant was desorbed by Si flux at 750°C in the case of sample A. On the $CoSi_2$ layer, a 5.0-nm-thick Si layer was grown at 200°C with As flux for

dopant using a valved cracking cell followed by a growth of 0.9-nm-thick CaF_2 layer. Subsequently, a 2.5-nm-thick CdF_2 quantum-well layer, a 0.9-nm-thick CaF_2 layer and finally the 0.9-nm-thick Si layer were grown at 80°C. After unloaded from the UHV chamber, Al/Au electrodes of 200 μm square were formed by lift-off.

4. Results and discussions

In the measurement of I-V curve shown in Fig. 3, bipolar resistance switching cycles have been clearly observed at room temperature for both sample A and B. However, stability and reproducibility of I-V curve were significantly different from each other. Switching voltage V_{peak} (from low resistance state to high resistance state) for sample A was 0.67 V and ON/OFF current ratio was around 10. On the other hand, V_{peak} for sample B was distributed widely from 0.8–1.3 V and ON/OFF ratio was distributed in the range of 2–20. These results strongly imply that high-quality interfaces between $CoSi_2$ and Si have been obtained for sample A because protective oxide layer for surfactant suppressed agglomeration and segregation of Co during the thermal silicidation processes, which has improved interface quality of quantum-well heterostructures [9].

5. Conclusion

We have investigated fabrication technique of resistance switching diode using $Si/CaF_2/CdF_2/CaF_2/Si$ heterostructures on $CoSi_2$ layer as low resistance lead line. It has been found that introduction of protective oxide layer during Co silicidation significantly improves stability and reproducibility of I-V characteristics of the diode.

Device concept and fabrication technique proposed in this study is one possible candidate for new nonvolatile memories or ReRAM elements for the future LSI technologies toward ultimate scaling in nanometer scale.

References

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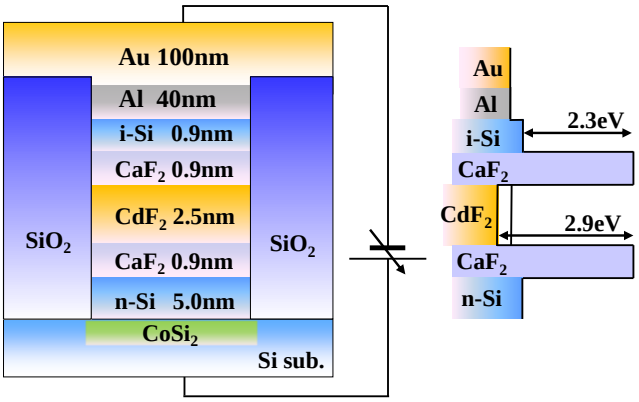

Fig. 1 Schematic device structure and conduction band profile.

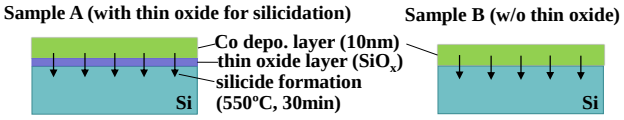

Fig. 2 Schematics of formation process of $CoSi_2$ layers for sample A and B.

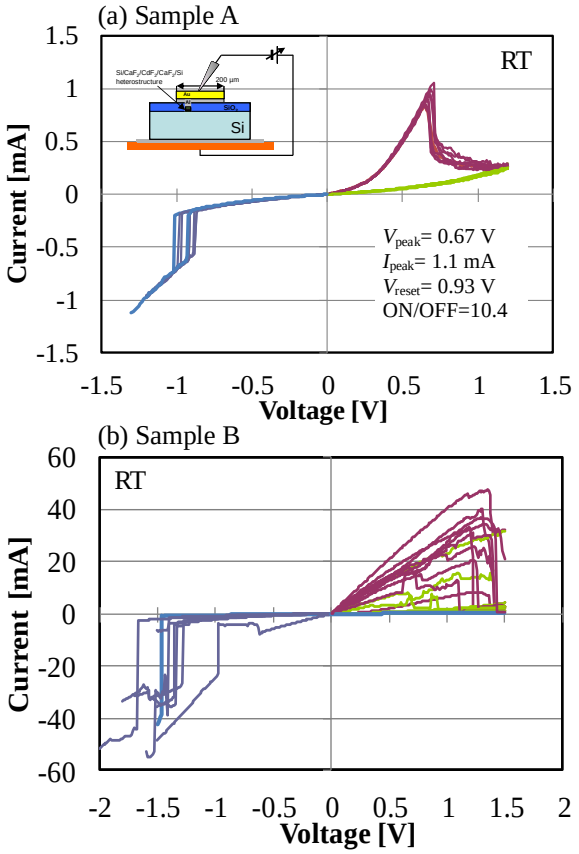

Fig. 3 I-V curve at room temperature exhibiting bipolar resistance switching operation for cyclic set/reset bias sweep. (a) for sample A (with thin oxide during the silicidation) and (b) for sample B (w/o thin oxide).