

## An Investigation on GIDL Mechanism of Program Disturbance in Sub-20nm NAND Flash Memory

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### Abstract

Disturbance induced by GIDL are investigated. A new program disturbance phenomenon by boosted channel potential lowering by GIDL is found. In addition, temperature dependency of the disturbance by GIDL is measured. Finally, the structure and bias conditions to overcome the GIDL are suggested.

### 1. Introduction

NAND Flash memory has been successively achieved its primary goal of expanding capacity by scaling the cell size and adopting multi-level NAND cells including MLC and TLC [1]. However, as the device shrinks to sub-20 nm, extremely more efforts than ever before are required to fulfill the criteria such as distribution, reliability, and performances even with technological aids from algorithms and controller solutions like ECC engine. One of the most crucial problems impeding robustness in scaled device is disturbance, and several articles pointed out that disturbance are strongly affected by hot carrier injections because of gate-induced drain leakage (GIDL) [1,2].

In this paper, we elucidate degradation of disturbance by GIDL and its temperature dependency. From the results, methods for increasing the immunity to GIDL are proposed.

### 2. Experimental results

Program (PGM) disturbance means unintentional positive  $V_{th}$  shift in erased cells under PGM bias on WL and boosted potential on channel as shown in Fig. 1. Appropriate boosted potential levels are needed to suppress the PGM disturbance because high boosted potential as well as low level of it could cause disturbance. As boosted level is escalated, although FN tunneling is restrained, the amount of hot carriers led from horizontal and vertical E-field severely increases and edge word lines (WLs) are susceptible to be degraded by hot carrier injection (HCI) into floating gate. In particular, hot carriers by vertical E-field in overlap region of junction and gate are called GIDL-induced hot carrier.

At first, we compared the disturbance characteristics with various gate bias levels of Source Select Transistor (SSL) to confirm the GIDL-induced disturbance in 1x nm devices. Global boosting scheme is used, all cells are erased, and PGM bias applied to WLs is fixed to same range to eliminate additional pulses by lowered PGM speed due to SSL bias. Disturbed  $V_{th}$  of erased cells in Fig. 2 greatly decrease with higher SSL bias, and three details are founded as follows. First, GIDL is the dominant cause of disturbance rather than punch through in SSL. Moreover, GIDL in SSL affects

entire boosted potential level even in farthest WL63, whereas HCI directly into neighboring floating gate was considered the only degradation mechanism for the GIDL induced disturbance [1,2]. This is attributed to the fact that parts of the electron-hole pairs (EHPs) engendered by GIDL leak to other electrodes like gate or substrate due to potential differences and consequently entire boosted level in a NAND string is lowered as illustrated in Fig. 3. Finally, temperature dependency of SSL effects is founded.

To verify the GIDL induced entire boosted potential drop, disturbance in WL63 is repeatedly measured with different SSL bias and back patterns as shown in Fig. 4. SSL bias effects on suppressing GIDL current observed only in the all erase pattern. This implies that boosted potential is naturally localized by already programmed WLs that cut off the potential in NAND string even with high pass bias due to shallow doping concentration in S/D junction and reduced fringing field by adopting a structure with air-gap. In this self-localized boosting mode, the SSL bias could not influences on GIDL current occurring at cut-off WLs.

SSL bias effects on disturbance showed an temperature dependency as mentioned in Fig. 2; the effects attenuate at high temperature. In order to examine intrinsic properties of GIDL current in SSL, I-V curves of SSL are measured as shown in Fig. 5 (a). Leakage current by GIDL is detected in the range of off-state of transistor and it is increased at higher drain(=BL) bias. On top of this, in Fig. 5 (b), GIDL leakage has strong relationship with temperature at low E-field, however, the dependency gradually fades away at high E-field. This is ascribed that at low E-field EHPs are predominantly generated by Shockley-Rheed-Hole (SRH) model which depends on temperature, while at high E-field EHPs are mainly formed by Band-to-Band Tunneling (BTBT) model that is insensitive to temperature [3]. Thus, Even if E-field is considerably repressed by SSL bias in Fig. 2, the improvement of disturbance is only remarkable in low temperature because of temperature dependency of GIDL.

### 3. Discussions

GIDL deteriorates disturbance characteristics of NAND cells by dropping entire boosted level in the string as well as HCI as mentioned above. Because contour and intensity of boosted potential, especially in the edge area, plays a key role to decide GIDL induced disturbance, graded potential by manipulating WLs bias or back patterns of each cell is an excellent manner to alleviate GIDL as measured in Fig. 6. However, in scaled device, because boosted potential is unintentionally localized wherever cells with high  $V_{th}$  exist, graded potential restricted in edge area cannot help showing

limited effects. Moreover, as it is difficult to fix and control the cut-off WLs in self-localization, the degree of fluctuation is raised among individual NAND strings. Thus, it should be contended that cell structures without getting self-localized by patterns is essentially needed and GIDL suppressing schemes such as SSL bias or graded potential contour must be added to the structure.

Furthermore, the method to soothe disturbance at high temperature should be considered because the ways decreasing E-field mentioned above simultaneously worsen temperature dependency. In other words, disturbance in high temperature cannot be resolved by adjusting bias conditions and it is radically required to reduce trap-site in overlapped area of junction and gate for curbing SRH processes.

#### 4. Conclusion

In this paper, disturbance caused by GIDL are described. It is founded that GIDL can degrade the entire boosted potential in NAND string and has strong dependence on temperature at low E-field due to EHPs generation by SRH mode. Finally, to suppress GIDL, graded potential and the structure without self-localization is suggested.

#### References

- [1] I.-H. Park, *et al.*, VLSI Tech. Dig., pp. 23-24, 2012. [2] J.-D. Lee, *et al.*, IEEE NVSMW, pp.31-33, 2006. [3] M. Rosa, *et al.*, IEEE TED, vol. 47, pp. 154-159, Jan., 2000

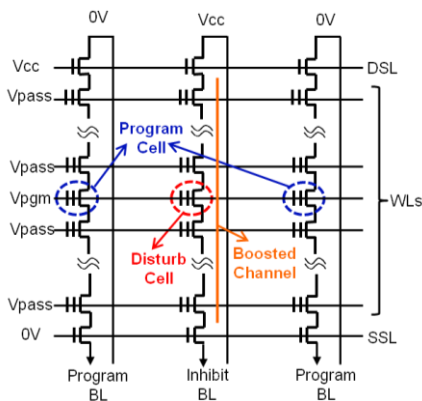


Fig. 1 Schematic of NAND cell array. PGM disturbance occurs in cells under high PGM bias in inhibited BLs. Both low and high boosting potential can bring to worsen disturbance characteristics.

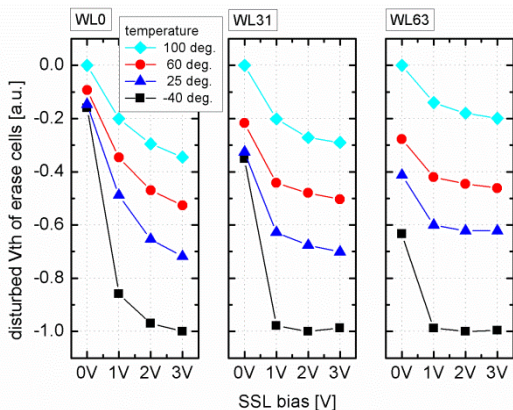


Fig. 2 Vth of erased cells after PGM operation with various SSL bias and temperature. The Vth shift is improved by increasing SSL bias especially in low temperature.

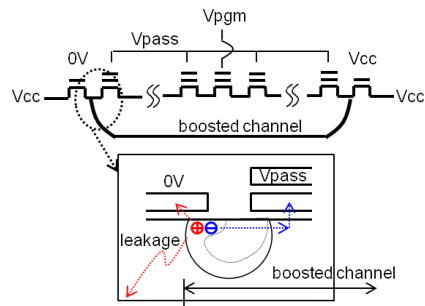


Fig. 3 Schematic of GIDL effects on disturbance. Hot electrons generated under GIDL conditions are allegedly injected into neighboring cells [2]. Also, it is founded that entire boosting level is dropped by GIDL which is ascribed to the leakage current toward substrate and gate of SSL.

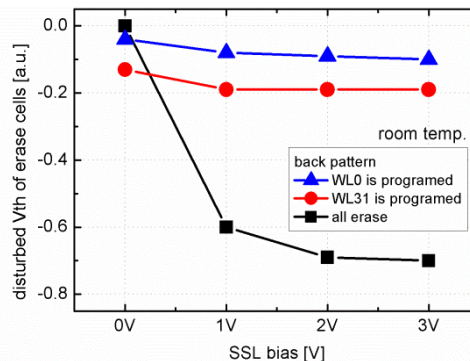


Fig. 4 Vth of erased cells after PGM operation with a plethora of SSL bias and back patterns. The effects of SSL bias are vanished in programmed back patterns due to self-localization.

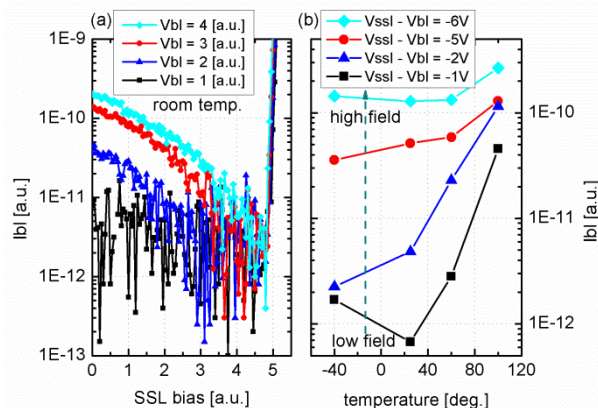


Fig. 5 (a) I-V curves of SSL. Leakage current by GIDL is detected with various drain(=BL) bias. (b) Temperature dependency of GIDL current. As E-field lowers, the dependency becomes stronger due to increasing portion of EHPs by SRH process.

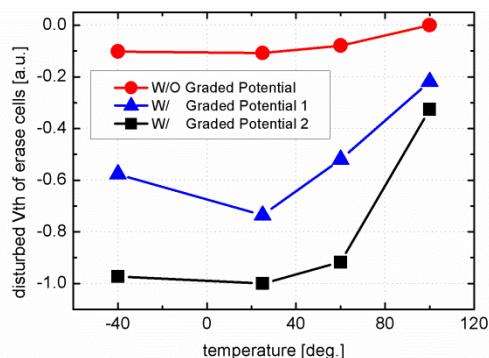


Fig. 6 disturbed Vth of erased cells with and without applying graded boosting potential. The disturbance property is improved by using Graded boosting contour.