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A Novel Approach for the Understanding of the Charge Loss Paths in a SONOS Flash Memory

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Abstract- The application of the three-level charge pumping technique to the SONOS flash memory has been demonstrated. It has been applied toward the understanding of the charge loss mechanism in a flash memory cell. Two different programming schemes have been used to demonstrate the efficacy of such a method. A 2 bit/cell operation has been demonstrated for this purpose. It was found that the three-level CP can be used to identify the fast traps which are directly related to the charge loss in a SONOS cell.

Introduction- In a SONOS cell, the program and/or erase operation are achieved by the tunneling of electrons/holes through the **thin** tunnel oxide such that it will induce the oxide damage, either in the form of oxide traps (fast traps) or interface traps (fast traps). Both traps contribute to the charge loss leakages [1]. In the past, SILC or two-level charge pumping measurement is popular to observe the leakage components through either traps. Further techniques still need to be developed for the understanding of the charge loss mechanism in relating to the data retention.

In this paper, an improved three-level charge pumping technique has been implemented to measure the traps, especially the fast traps, in a SONOS cell. Two different programming techniques on a 2-bit/cell SONOS have been used to examine the correlation of these generated fast traps to the charge loss.

1. Device Preparation

The n-channel flash cells with ONO thickness (50/60/50) (A^o), W/L=0.2/0.22(um), were fabricated using standard 0.13um CMOS technology.

2. Principle of the Three-Level Charge Pumping

The schematic of a three-level CP, 3CP, improved from [2], is shown in Fig. 1(a), with the gate pulse in Fig. 1(b). There are three levels, V_{high}, V_{mid} and V_{low}, where V_{high} is higher than the threshold voltage, V_T, and V_{low} is lower than the flat-band voltage, V_{FB}. In a conventional two-level CP, a square pulse with V_{high} and V_{low} is applied at the gate while the channel is switched between accumulation and inversion, from which the current measured from the substrate is called CP current, I_{CP}. For a 3-level CP, an additional level V_{mid} is added between V_{high} and V_{low}. By varying the holding time, more trap properties can be detected. The measured CP current by the 3-level CP method as holding time varies, is shown in Fig. 2, in which the holding time was varied from 0 to 250nsec and the results can be divided into four regions. The regions of interest in our study is region (1) and (2), in which region I is similar to two-level CP measurement and region II is for fast trap measurement.

3. Applications to Two-Different Operating Schemes

To explore the generated traps in a SONOS cell, two different programming schemes, CHEI (Channel Hot-Electron Injection) and FBEI (Forward Bias Electron Injection) were studied [3-4], Figs. 3, 4 and Table 1. The erase was done by BBHH [4]. The programming scheme, FBEI, by the authors in [4], consists of two steps of electron injection. Initially, electrons are injected from the drain into the substrate under a forward bias. Then, electrons are turned back and accelerated toward the interface by an applying positive gate bias and finally jumped over the bottom oxide, reaching the nitride layer via the vertical field. The 3CP measurements were carried out on the cells after going through the cycling by these two programming schemes.

From Fig. 5, two major results can be obtained from the comparison of Figs. 5(a) and 5(b), i.e., (1) in region I, CHEI generate larger interface traps (Nit), and (2) in region II, the slope changes in show significant differences. It can be justified from Figs. 6(a) and (b) in which the generated fast traps at the interface in CHEI (solid squares) has faster generation rate than the FBEI ones (solid circles), as cycling progresses. As a consequence, after very long term P/E cycles, CHEI scheme induces much worse oxide degradation from the traps in both region I and region II.

4. Comparison of the Charge Loss

The correlation between the trap generation and its dependency on two different schemes can be understood from Fig. 7, the band diagram of the SONOS cell, after the cycling. Three paths for the electron injection [5] are shown. Path (3) is the direct tunneling. Path (2) is the tunneling of electrons via trap-assisted tunneling. Path (3) is related to the generation of fast traps at the interface, N_{it}. Path (1) is the path for electron thermionic emission [6], which allows the electrons to jump over the oxide without causing any traps. It is most likely that more slow traps, N_{ot}, and fast interface traps, N_{it}, were generated for CHEI through paths (2) and path (3) respectively. While, FBEI has more chances for its carriers to follow path (1). In short, from the 3CP measurement, fast traps can be measured and are responsible for the charge loss during the cycling. In CHEI, more $N_{it's}$ were generated, while, FBEI will favor the electrons to be injected via the thermionic emission without creating additional traps, since the electrons in this scheme exhibit higher kinetic energy. Therefore, under the same P/E cycles utilizing FBEI or CHEI, the former cause less degradation at the bottom oxide, which shows that FBEI demonstrates better reliability than CHEI. To justify the above arguments, the data retention after 10k P/E cycles for two different schemes is compared in Fig. 8. After 10 years, the threshold voltage window is larger for FBEI scheme, i.e., less charge loss was observed for this scheme. This charge loss experiment confirms that less oxide damage was created at the bottom oxide in FBEI scheme.

In summary, a new application of three-level CP on the study of interface trap generation in a SONOS memory cell has been demonstrated. Tested against different programming schemes, the generation of fast traps at the bottom oxide of SONOS after P/E cycles, the charge loss behavior can be well understood and its correlation to the data retention can be verified. It has been successfully verified that FBEI indeed exhibits better data retention through this specially designed three-level CP measurement technique.

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Functions	Schemes	P/E time	Gate Bias	Drain Bias
Program	CHEI	1msec	V_G= 6V	4.5V
	FBEI	1msec	V_3= 6V	V_2= 4.5V V_1= -1V
Erase	BBHI	10msec	V_G= -9V	4.5V

Table 1 The operating conditions of the two tested programming schemes and the erase operation.

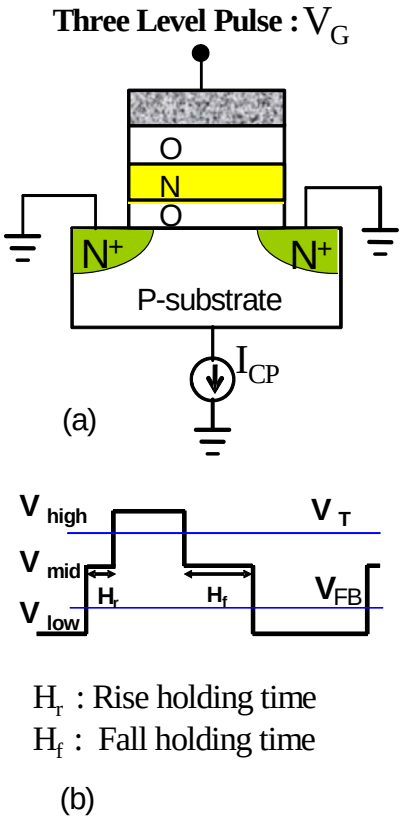


Fig. 1 (a) The schematic of the three-level charge pumping measurement. (b) The pulse waveform with a varying holding time. When H_f is very small, fast traps can be measured.

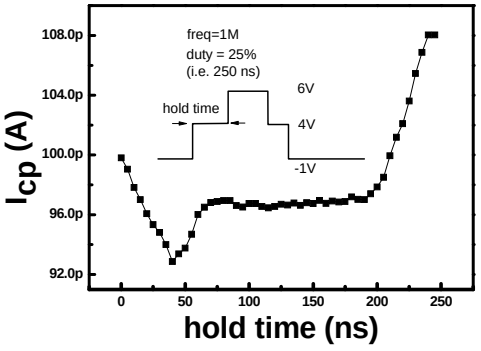


Fig. 2 Measurement results of the charge pumping current as a function of holding time.

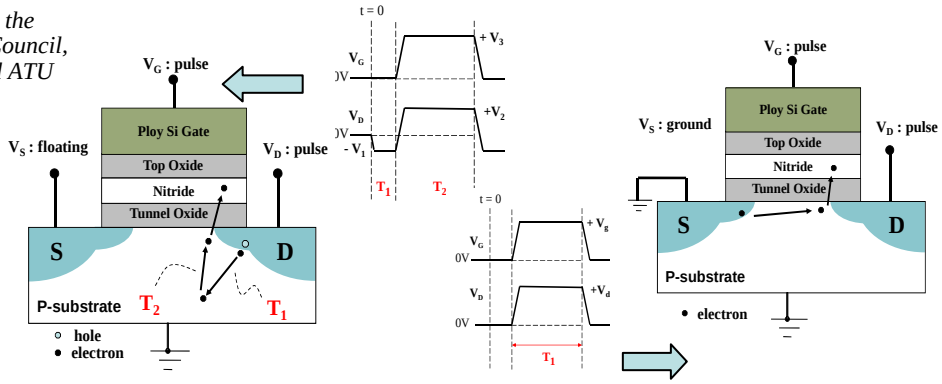
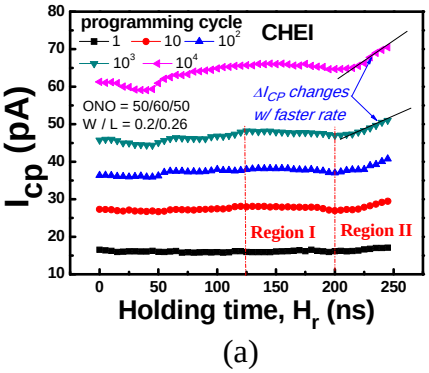
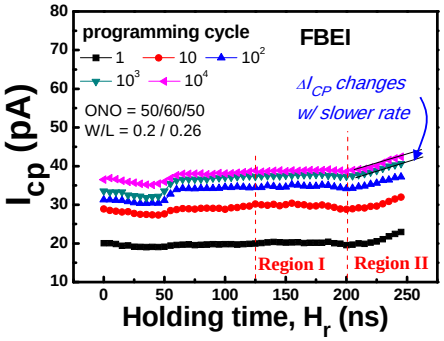


Fig. 3 Experimental set up and timing diagram for FBEI (Forward-Bias assisted Electron Injection).

Fig. 4 Experimental set up and timing diagram for CHEI (Channel Hot Electron Injection).

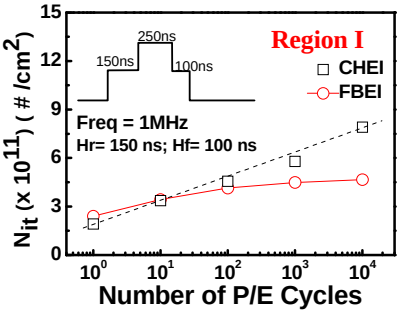


(a)

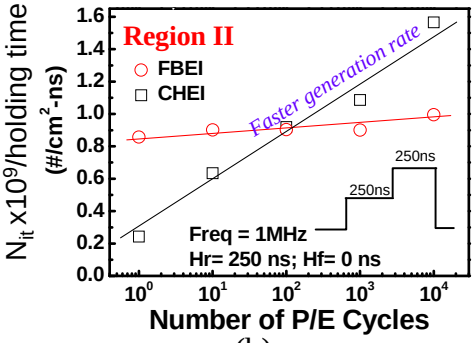


(b)

Fig. 5 The measured three-level I_{CP} currents as a function of holding time, after the P/E cycles, (a) Operating by the CHEI scheme, (b) Operating by the FBEI scheme.



(a)



(b)

Fig. 6 (a) The calculated interface traps as a function of cycling time in region III. (b) The changing rate of the traps for two different schemes in region IV. Note that CHEI exhibits a faster generation of the fast traps.

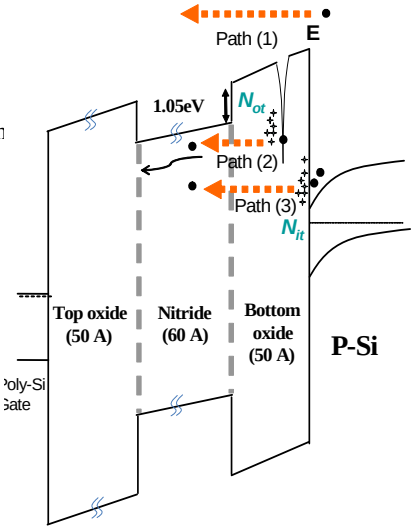


Fig. 7 The energy band diagram used to explain the charge leakage paths in a SONOS cell. Paths (1)(2) are dominant in FBEI scheme. Paths (2) and (3) are dominant in CHEI scheme.

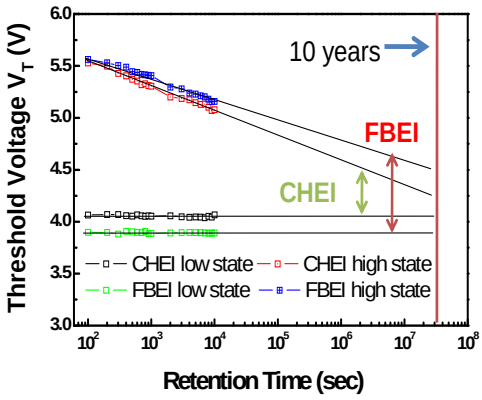


Fig. 8 The data retention measurement for two different schemes. 2-bit operation of the SONOS were performed. Predicted from a 10 year lifetime, FBEI scheme shows much less charge loss than the CHEI ones, which is consistent with the lower generation rate of FBEI in Fig. 6.