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A New Lateral Conductive Bridge Random Access Memory (L-CBRAM) by Fully CMOS Logic Compatible Process

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ABSTRACT

A novel fully-logic compatible Lateral CBRAM has been demonstrated by a sidewall Ti-atomic switch between poly-Si and a CMOS logic regular contact plug, the lateral Ti-based sandwich CBRAM structure can be well turned on or off at 1mA/1.5V by bipolar switching operations. More than 5X On/Off resistance ratio is successfully achieved after more than 1,000 pulse cycles, and it also has very stable data retention at high temperature. The innovative Ti-based Lateral CBRAM (L-CBRAM) is a very promising solution for future embedded MTP applications.

Introduction

The scaling of embedded NVM cell is becoming very difficult because of the thickness limitation of floating gate oxide. Conductive Bridge Random Access Memories (CBRAM), also called Programmable Metallic Cells (PMC) or electrochemical memory (ECM), is noticed for the advantages of scalability, fast operation speed and low power consumption [1-3]. Commonly, the structure of CBRAM is formed by a stacked structure of an active electrode, electrolyte, and an inert electrode. The active electrode is acting as an ion supplier to form a conductive bridge into the electrolyte. The active electrode usually uses Cu and Ag and the other electrode must be inert to reaction as Pt & W. The electrolyte materials can be oxide [4] or chalcogenides [5]. Since the principle mechanism of CBRAM is using Cu or Ag ions to form and dissolve the filaments[6]. In this work, a new Ti-based lateral CBRAM is proposed and demonstrated instead of vertical stacked method for high density embedded NVM applications. The new CBRAM does not need a complicate or CMOS incompatible stacked structure for electrolyte formation, we firstly proposes to use Ti atomic layers, which is existing in general CMOS logic contact plug, to form and to rupture the metal filaments by a bipolar switching operation. Moreover, the new Lateral CBRAM has been successfully fabricated and demonstrated by TSMC 0.18um CMOS logic technology without any extra process and masking step.

Characterization and Discussion

The sidewall CBRAM is structured by a composite Ti/TiN barrier layer from CMOS logic contact process, the cell contact is processed to slightly overlap on one side of a poly gate to form a side-by-side structure of lateral CBRAM, where the poly gate is acting as an inert electrode of CBRAM. For a regular CMOS contact, there is a composite barrier layer of Ti/TiN before W deposition, the Ti of the composite layer is for the switching atom and the TiN layer and the later W plug is the active electrode. The schematic and TEM of the lateral CBRAM cell is illustrated in Fig.1. Where the resistive switching part is located at the lateral region of W/TiN/Ti/Poly-Si between Contact-plug and Poly-gate. Fig.2 further shows the laterally atomic switch model of the Lateral CBRAM. Initially, The Lateral CBRAM has a lateral connection of the Contact-plug and Poly-gate and showing a lower resistance. In Reset forming operation, the connection of Ti metal is rapidly ruptured by high current density and local heat. The Ti atoms are pushed away to one side and disconnect the original conductive path for reaching a higher resistive state. In following Set operation, the Ti atoms are pushed back to reconnect the path and regain a lower resistance state. Fig.3 indicates the current flows through a lower resistive state by a Ti-metallic connection and the remained small off-state current could be caused by the trap-assisted tunneling leakage. Fig.4 shows the basic I-V characteristics of the new Lateral CBRAM. A high forming current of 6mA is required to break the initial Ti-based sidewall structure, and the voltages of set and reset are -1V and 1.5V, respectively. Furthermore, the current level of initial state is higher than the following On-states by a set current compliance and illustrated in Fig.5. Besides, when we increase the compliance current, the reset current will be increased accordingly because of the Ti conductive bridge becoming thicker as shown in Fig.6. Time to Set and Reset are characterized and shown in Fig.7, where the reset time(5ms) is much longer than the set time(50ns) due to it's relatively difficult to break a physical Ti-atomic bridge than to form a tiny filament. In reliability analysis, the switching cycling of MTP level has been characterized and shown in Fig.8. Furthermore, there is no read disturb concern for 10,000 seconds as shown in Fig.9. The data retention characteristic is shown in Fig.10. There is no conductive bridge state shift after 1000hours bake at 150C. Finally, the characteristics of the Lateral CBRAM (L-CBRAM) is summarized in Fig.11.

Conclusion

In this paper, a new CMOS logic compatible Lateral CBRAM (L-CBRAM) is firstly proposed and successfully demonstrated in pure CMOS logic process. The laterally bipolar resistance switch between contact and poly has been accomplished without additional materials, process step, or mask. The new Lateral CBRAM (L-CBRAM) will be a promising candidate of future logic NVM solutions.

Reference

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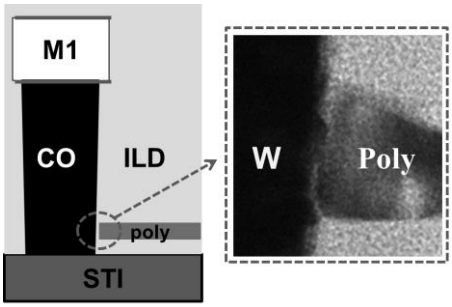

Fig.1. Structure Schematic and TEM analysis of Lateral CBRAM (L-CBRAM) cell.

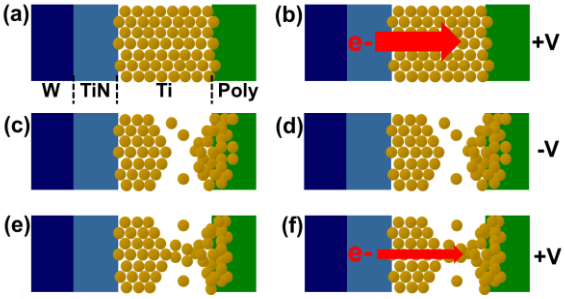

Fig.2. The illustration of reset/set mechanism. (a)initial state (b)first reset (c)off-state (d)set (e)on-state (f)normal reset.

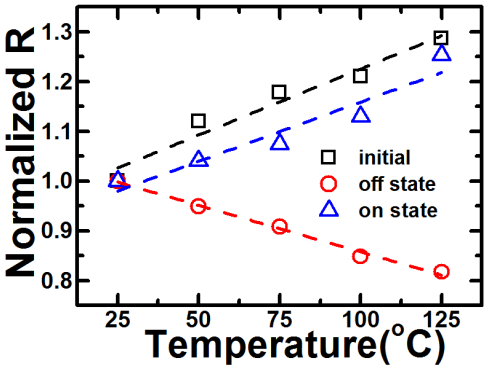

Fig.3. Resistance of Initial/On/Off states at different temperatures.

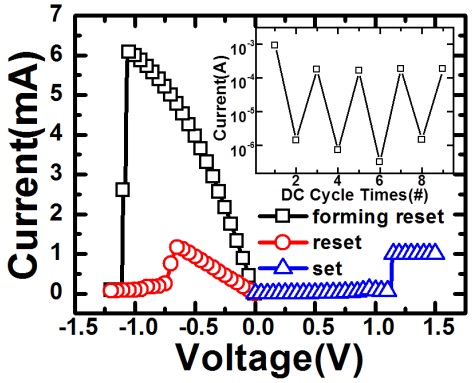

Fig.4. Reset and Set characteristic for bipolar operation and the first several states of DC cycle is shown in inserted diagram.

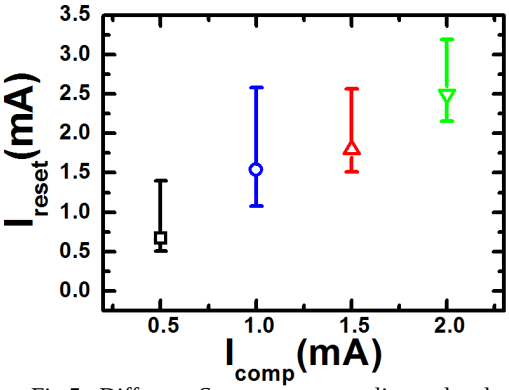

Fig.5. Different Set current compliance levels for different Reset current.

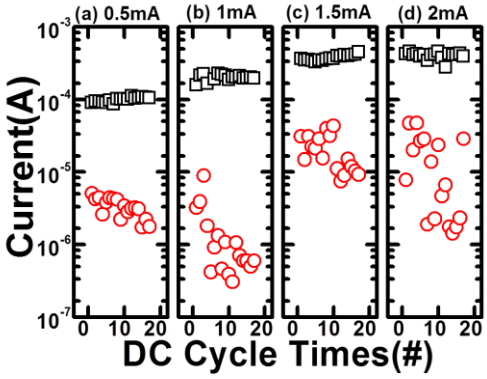

Fig.6. Read current level and On/Off window in different Set current compliance.

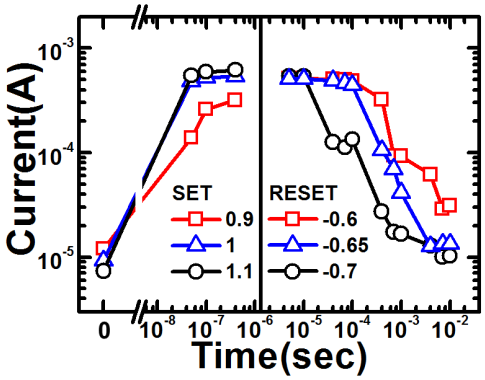

Fig.7. Time to Set and Reset of the new Ti-based Lateral CBRAM (L-CBRAM) in different voltages.

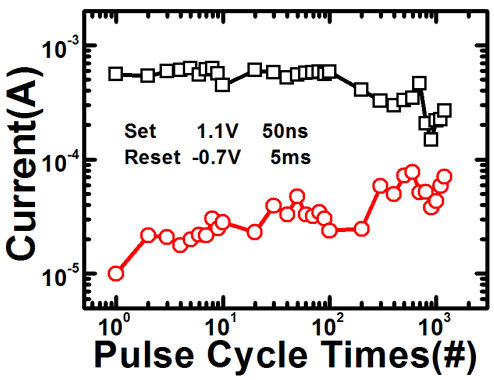

Fig.8. L-CBRAM cycling test for Reset at -0.7V/5ms and Set at 1.1V/50ns. The 5X On/Off ratio is remained after 1k cycles.

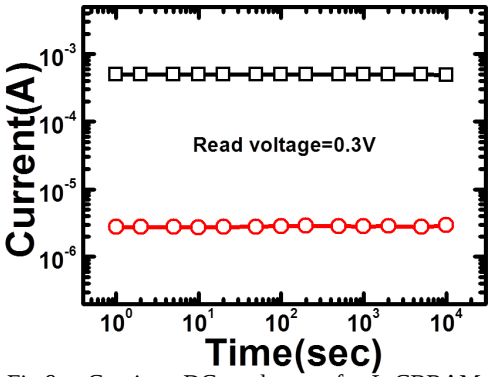

Fig.9. Continue DC read stress for L-CBRAM, the resistance level is stable after 10k sec.

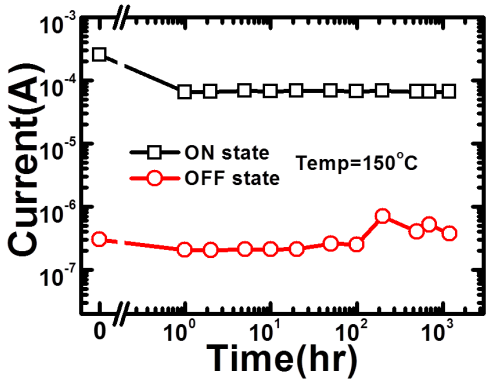

Fig.10. Ti-atomic switching states are not shifted under 150°C for 1000 hours.

lateral CBRAM		
memory node		W/TiN/Ti/poly
switching type		bipolar
operation condition	read	0.1V
	forming	-1V / ~6mA
	reset	-1V / >1mA
	set	1.5V / 1mA
speed	reset	5ms
	set	50ns
cycling times		1000
on/off ratio		>5

Fig.11. Characteristic summary of the new Lateral CBRAM (L-CBRAM).