Extended Abstracts of the 2013 International Conference on Solid State Devices and Materials, Fukuoka, 2013, pp540-541

Excellent Scalability Including Self-Heating Phenomena of Vertical-Channel Field-Effect-Diode (FED) Type Capacitorless One Transistor DRAM Cell

Takuya Imamoto[1, 2] and Tetsuo Endoh[1, 2]
[1] Graduate School of Engineering, Tohoku University, [2] JST-CREST
Aramaki aza Aoba 6-6, Aoba-ku, Sendai, 980-8579, Japan
Phone: +81-22-795-4401 E-mail: tetsuo.endoh@cies.tohoku.ac.jp

Abstract

The excellent scalability of the vertical channel Field Effect Diode (FED) type 1T-DRAM including Self-Heating Effect (SHE) is presented for the first time. The vertical channel FED type shows the excellent hold characteristics (100msec at 358K) even when silicon pillar diameter is scaled down to 12nm. Moreover, we also show that by employing the vertical FED type, increase of lattice temperature due to SHE (ΔT_L^{Max}) can be suppressed to a negligible small value of 0.6K.

1. Introduction

Capacitorless 1T-DRAM was proposed to overcome the scaling limitations of conventional 1T-1C DRAM [1]. Previously, we proposed the low power vertical channel FED type 1T-DRAM with Negative Hold Bit line (NHB) bias scheme for excellent retention and read disturb characteristics [2]. On the other hand, SHE in non-planar FETs becomes worse than those of conventional bulk planar MOSFETs [3]. In this paper, we show the excellent scalability of vertical channel FED type 1T-DRAM. Moreover, we also show the excellent thermal properties of FED type 1T-DRAM by comparing with the Bipolar Junction Transistor (BJT) type via 3-dimensional device simulator [4].

2. Memory Cell Operation of Vertical-Channel FED Type 1T-DRAM Cell

Figure 1 (a) shows the schematics of the vertical channel FED type 1T-DRAM cell (vertical FED type). In the vertical FED type, Bit Line (BL), Word Line (WL), common Control Gate (CG), and Source Line (SL) are located vertically. Therefore, an ideal cell size of $4F^2$ can be achieved. Simulated memory cell design parameters and operation voltages are shown in Table I. Figure 2 shows the BL current ($|I_{BL}|$) versus BL voltage V_{BL} characteristics for three different WL voltages (V_{WL}) of vertical FED type with 20nm silicon pillar diameter (D). As the V_{BL} is increased in negative, $|I_{BL}|$ increases sharply at a point which is determined by V_{WL} Moreover, $|I_{BL}|$-V_{BL} curve shows hysteresis when V_{BL} is swept back to 0.0V. Memory cell operation of the vertical FED type (D=20nm) at 300K is shown in Fig. 3 (a) and (b). Data can be written and read within 20nsec access time. The current of write "1" and "0" are 3.77μA/cell and 0A/cell. The current of read "1" and "0" are 2.45μA/cell and 5.85pA/cell.

3. Memory Cell Performances and Scalability of Vertical-Channel FED Type 1T-DRAM Cell

The retention and read disturb characteristics of the vertical FED type (D=20nm) are shown in Fig. 4(a) and (b). The vertical FED type shows 2,000msec retention time and 100msec read disturb characteristics at 358K. In the read disturb characteristics, each node voltages except for V_{BL} are set to "Hold" and V_{BL} is set to "Read" in Table I (a). Figure 5 and Fig. 6 show the scalability of the vertical FED type. The vertical FED type shows the excellent hold characteristics (100msec at 358K) with large enough read current margin (1μA/cell) even when D is scaled down to 12nm. From all, it is shown that the vertical FED type 1T-DRAM cell has an excellent scalability.

4. Evaluation of SHE in 1T-DRAM Cell with Difference Structure and Operation Principle

To evaluate SHE of 1T-DRAM cell, Write "1" operation with difference structures (bulk vertical or SOI planar) and operation principles (FED or BJT) as shown in Fig. 1 (a) and (b) are calculated. Table II shows operation voltages and design parameters used in this study. Figure 7 (a) and (b) show the time dependence of maximum lattice temperature in the memory cell (T_L^{Max}) and $|I_{BL}|$ of FED and BJT type with different structure. In the FED type, both bulk vertical and SOI planar structure show negligibly small SHE, and the peak value of T_L^{Max} is 300.6K for bulk vertical and 300.4K for SOI planar. This is because FED type 1T-DRAM can operate low voltage (-1.1V) while BTJ type needs high V_{BL} (2.0V) to trigger impact ionization. Therefore, FED type shows excellent thermal characteristics. On the other hand, in the BJT type, T_L^{Max} is 330.6K for bulk vertical and 357.8K for SOI planar. Moreover, in the FED type, $|I_{BL}|$ increases sharply when BL is applied while in the BJT type increases gradually. Figure 8 shows the peak value of T_L^{Max} during Write "1" operation in the bulk vertical FED type as a function of the D. Even when D is scaled down to 12nm, the peak value of T_L^{Max} is constant value of 300.6K and shows negligibly small SHE. Table III shows the comparison of memory performances.

5. Conclusions

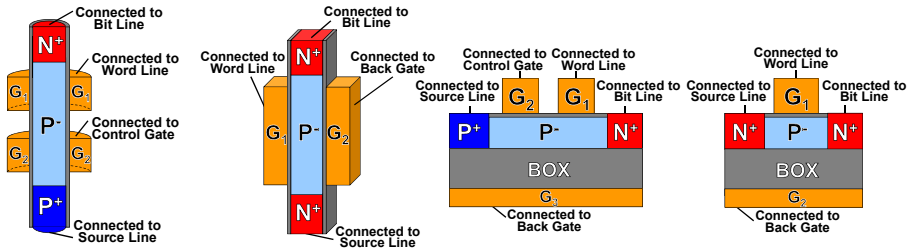
The excellent scalability of vertical channel FED type 1T-DRAM cell considering thermal characteristics is presented for the first time. The vertical FED type shows the excellent hold characteristics (100msec at 358K) with large enough read current margin (1μA/cell) and negligibly small SHE (T_L^{Max}=300.6K) even when D is scaled down to 12nm.

Acknowledgements

This work has been supported in part by a grant from "Research of Innovative Material and Process for Creation of Next-generation Electronics Devices" of CREST under the JST.

References

[1] T. Ohsawa, et al., *IEEE J. Solid-State Cir.*, p. 1510, 2002.
[2] T. Imamoto, et al., *Jpn. J. Appl. Phys.*, **52**, p. 04CD08-1.
[3] S. Kolluri, et al., *IEDM Tech. Dig.,* 2007, p. 177.
[4] Sentaurus ver.2012.06G [http://www.synopsys.com].
[5] M. H. Cho, et al., *Workshop on SNW*, 2012, p. 17.
[6] W. Kwon, et al., *Jpn. J. Appl. Phys.*, **49**, p. 04DD04-1.



(a) **Vertical FED [2]** (b-1) Vertical BJT (b-2) Planar FED (b-3) Planar BJT

Fig.1 The schematics of the Field Effect Diode (FED) type and the Bipolar Junction Transistor (BJT) type 1T-DRAM cells.

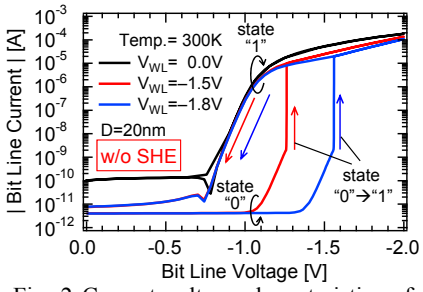
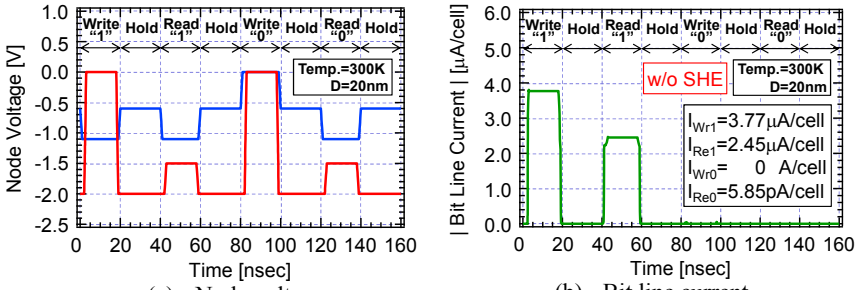


Fig. 2 Current voltage characteristics of vertical FED type 1T-DRAM cell. Steep and hysteresis characteristics are obtained (D=20nm).



(a) Node voltage (b) Bit line current

Fig. 3 Memory operation of the vertical FED type 1T-DRAM cell (D=20nm). Data can be written and read within 20nsec access time. The vertical FED type has a good current margin for Write/Read operation.

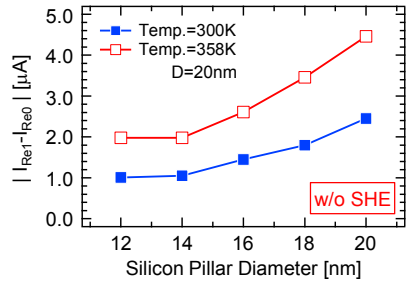
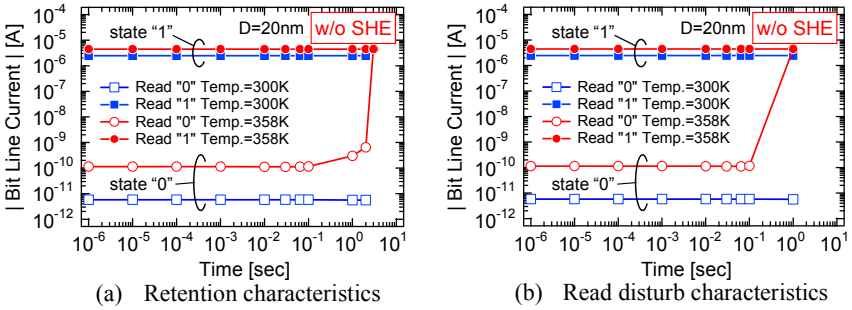


Fig. 5 Scalability of read current margin of the vertical FED 1T-DRAM cell. The vertical FED shows a good current margin even when silicon pillar diameter is scaled down to 12nm.



(a) Retention characteristics (b) Read disturb characteristics

Fig. 4 Retention and read disturb characteristics at 300K and 358K for the vertical FED type 1T-DRAM cell (D=20nm).

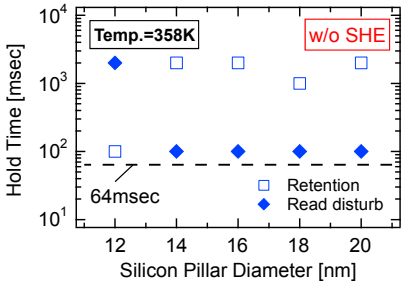
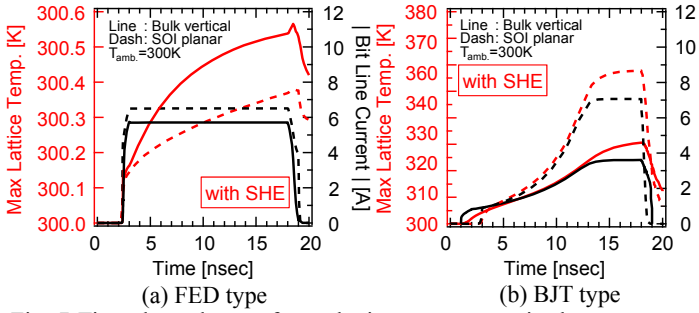


Fig. 6 Scalability of hold characteristics of the vertical FED type 1T-DRAM cell.



(a) FED type (b) BJT type

Fig. 7 Time dependence of max lattice temperature in the memory cell and bit line current of FED type and BJT type with difference of device structure. The FED type shows a negligible small change of lattice temperature.

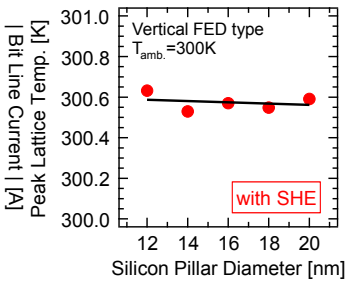


Fig. 8 Scalability of peak lattice temperature of the vertical FED type 1T-DRAM cell.

Table I (a). Memory cell design parameters

	Write"1"	Write"0"	Read	Hold
BL	-1.1V	0.0V	-1.1V	-0.6V
WL	0.0V	0.0V	-1.5V	-2.0V
CG	0.3V			
SL	0.0V			

Table I (b). Memory cell operation voltages

D	L_G	L_{CG}	T_{OX}	$V_{WL,Hold}$
20nm	60nm	50nm	5nm	-2.0V
18nm	60nm	50nm	5nm	-2.0V
16nm	50nm	40nm	5nm	-2.0V
14nm	40nm	30nm	5nm	-2.0V
12nm	30nm	20nm	5nm	-1.9V

Table II-(a). Memory cell operation voltages

	FED type		BJT type	
	Write"1" / Hold		Write"1" / Hold	
	Vertical	Planar	Vertical	Planar
BL	-1.1V / -0.6V	-1.1V / 0.0V	2.0V / 0.0V	
WL	0.0V/ -2.0V		-0.9V / -2.0V	
CG	0.3V			
BG		0.0V	1.0V	2.5V
SL	0.0V			

Table II-(b). Memory cell design parameters for SHE simulation

	FED type		BJT type	
	Vertical	Planar	Vertical	Planar
D, T_{Si}	20nm	20nm	20nm	9nm
L_G	60nm	60nm	50nm	20nm
L_{CG}	50nm	50nm		
T_{OX}	5nm	5nm	5nm	3nm
T_{BOX}		140nm		10nm

Table III. Memory performance comparison

	FED type		BJT type	
Structure	Planar	Vertical	Planar	Vertical
Wafer	SOI	Bulk	SOI	Bulk
Cell Size	>8F^2	4F^2	>6F^2	4F^2
I_{Re1}-I_{Re0}	1μA/cell	1μA/cell	1μA/cell	1μA/cell
Ret. Time (358K)	<0.1sec[2]	<2sec	<0.6sec[5] (300K)	<0.1sec[6]
ΔT_j^{Max}	0.4K	0.6K	57.8K	30.6K