

Fluorine ion implantation optimization in Saddle-Fin array devices for sub-40-nm DRAM technology

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Abstract

Fluorine (F) implantation with different dose post gate oxidation is used for investigating the performance of saddle-fin (S-Fin) array devices including gate-induced drain leakage (GIDL) and retention fail bit counts. Significantly lower retention fail counts of 35% were achieved in using a medium dosage of F implantation. Additional 18% retention fail count reduction was represented by F implantation with A degree tilt angle and 2X keV of energy. Trap passivation by F atoms in the source and the drain areas (S/D) could lead to the improvements.

1. Introduction

To catch up with Moore's law, the channel doping of a dynamic random access memory (DRAM) array device needs to be increased to help suppress the short-channel effects (SCEs). [1] The relatively high electric field of the junction leads to a shorter data retention, and higher leakage. In general, junction leakage, gated-induced drain leakage (GIDL), and interface states are the most dominant components of the leakage path for the retention time loss. To improve the leakage and retention time [2], structure optimization [1], asymmetric halo doping [3], and gate dielectric modification [4] were proposed. In this study, F implantation post gate oxidation was investigated with several experiments.

2. Experiments

Figure 1 shows a 3D schematic representation of the S-Fin device. After the recess channel patterning and etching, the gate oxide was grown using low-pressure wet oxidation and following additional F implantation. Most F dosage was kept at the top of the fin and the S/D verified by simulation. Since oxide thickness will be increased by F dosage, a decrease of oxide thickness in oxidation is performed to maintain in the same level. To make less impact of S-Fin oxide thickness by F implantation and to further investigate the location of trap passivation, the energy of X and 2X were designed to combine tilt angle of A and 2A.

3. Results and Discussion

The I_{DS} versus $(V_{GS}-V_{TH})$ curves of the S-Fin devices with different F dosage are shown in Fig. 2. In the case of F

implantation, GIDL is minimized from 10 to 20 times. The lowest GIDL is observed in medium F dosage.

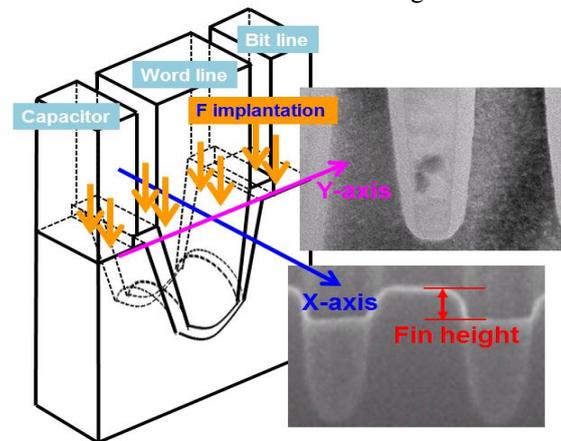


Fig. 1 S-Fin device schematic representation. The fin height for channel width and recess channel for channel length are shown in the TEM image of the X- and Y-axes, respectively.

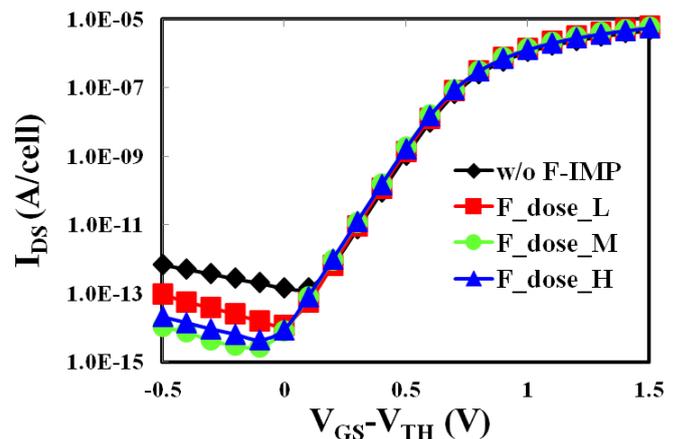


Fig. 2 I_{DS} versus $V_{GS}-V_{TH}$ curves of S-Fin devices. The lowest GIDL is observed in a medium dosage of F implantation.

Increase in effective oxide thickness (EOT), change of dopant profiles and trap passivation could be the mechanisms of GIDL improvement by using F implantation. V_T and time to breakdown (T_{BD}) increases with F dose as shown in Fig. 3. Therefore, the gate oxide thickness from tunneling electron microscope (TEM) picture shows thicker

oxide in top area of S-fin and no clear difference in sidewall area for all groups with different F dosage. The comparison is listed in Table 1.

Table 1 Comparison on gate oxide thickness of S-Fin device by TEM and normalized retention fail bit counts.

	w/o F	F dose L	F dose M	F dose H
S-Fin oxide thickness difference (%)	0	-1.9	+9.6	+11.8
Normalized retention fail bit counts difference (%)	0	-23.6	-34.6	-24.8

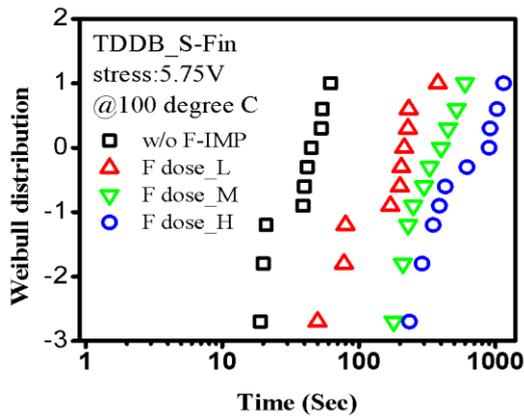


Fig. 3 Weibull distribution for time to breakdown of S-Fin devices. T_{BD} increases by F dosage results from oxide thickness increases.

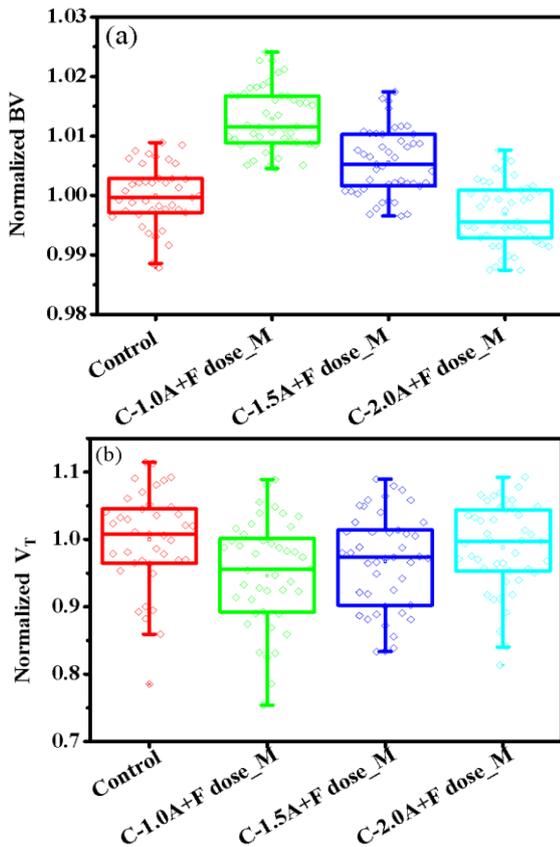


Fig. 4 (a) BV and (b) V_T of S-Fin devices with medium F dosage and different oxide thickness.

In the experiment of gate oxide thickness changes, electrical effective oxide breakdown voltage (BV) of a defined gate current and V_T distribution of S-Fin devices are shown in Fig. 4. No clear difference of retention fail bit counts and GIDL can be seen in all groups. It could be explained by electric field in sidewall oxide keep stable. However, a considerably high F dosage implantation results in damage and the corresponding retention fail bit counts increase, which is similar to the results by A. Weber et al. [5].

As shown in Fig. 5, the lowest normalized retention fail bit counts with 45% reduction compared to control samples is observed in 2X keV energy with A degree tilt angle, which could be explained F dose away from oxide interface and into Si area to passivate traps. The less impact in oxide thickness and S-Fin device from this tilted F implantation could be a potential candidate for retention performance improvement.

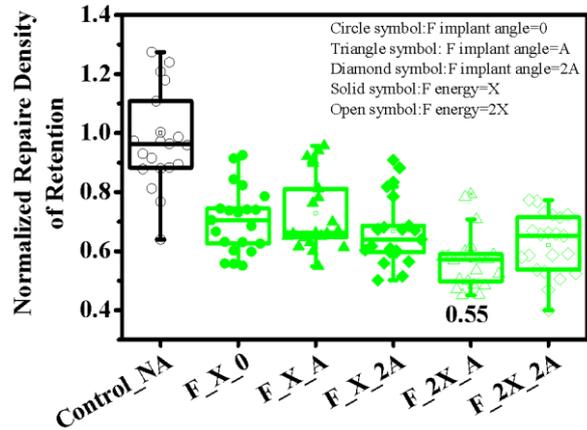


Fig. 5 Normalized retention fail counts of S-Fin devices with different energy and tile angle in F implantation.

4. Conclusions

Additional F implantation processed after gate oxide deposition in an S-Fin device was successfully demonstrated a reduction of 23.6 to 34.8%. The dosage of F implantation had a strong correlation with the retention performance, which could be mainly explained by the GIDL determined by trap passivation. Moreover, the F energy and tilt angle to control the location of the trap passivation in a high electric field area had been presented. The optimized condition for lowest normalized retention fail bit counts with 45% reduction is shown in the F implantation with energy of 2X keV and tilt angle of A degree.

Acknowledgements

This work was supported in part by the National Science Council of the Republic of China under contract number of NSC 101-2218-E-182-004.

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